

MOS INTEGRATED CIRCUIT

μ PD720112

USB2.0 HUB CONTROLLER



The μ PD720112 is an USB 2.0 hub device that comply with the Universal Serial Bus (USB) Specification Revision 2.0 and work up to 480 Mbps. USB2.0 compliant transceivers are integrated for upstream and all downstream ports. The μ PD720112 works backward compatible either when any one of downstream ports is connected to an USB 1.1 compliant device, or when the upstream port is connected to a USB 1.1 compliant host.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.
 μ PD720112 User's Manual: S16617E

FEATURES

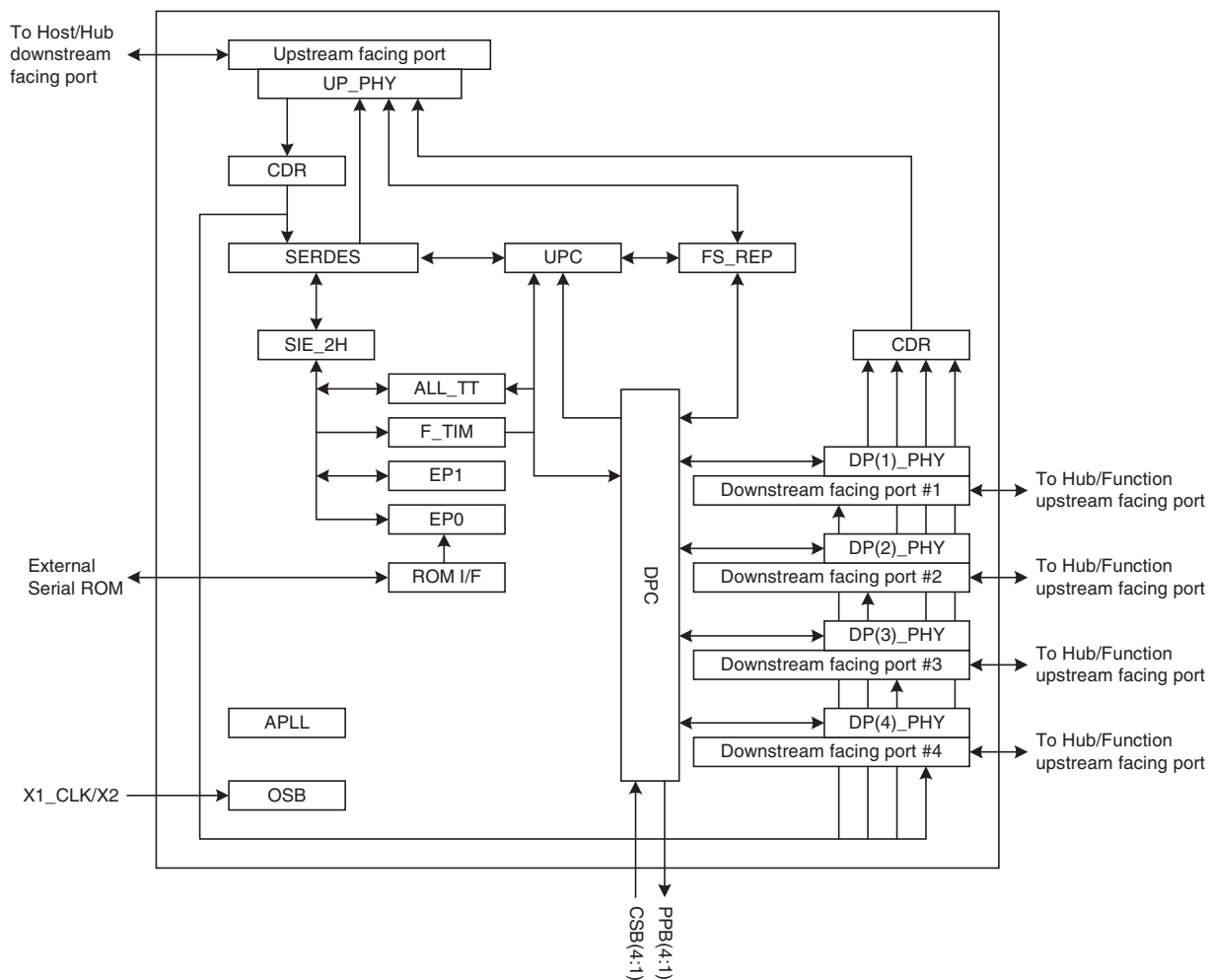
- Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 1.5/12/480 Mbps)
- Certified by USB implementers forum and granted with USB 2.0 high-speed Logo
- High-speed or full-speed packet protocol sequencer for Endpoint 0/1
- 4 (Max.) downstream facing ports
- All downstream facing ports can handle high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction.
- Supports split transaction to handle full-speed and low-speed transaction at downstream facing ports when Hub controller is working at high-speed mode.
- One Transaction Translator per Hub and supports four non-periodic buffers
- Supports self-powered and bus-powered mode
- Supports Over-current detection and Individual power control
- Supports configurable vendor ID, product ID, string descriptors and others with external Serial ROM
- Supports "non-removable" attribution on individual port
- Uses 30 MHz X'tal, or clock input
- Supports downstream port status with LED
- 2.5 V and 3.3 V power supplies

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

ORDERING INFORMATION

Part Number	Package
μPD720112GK-9EU	80-pin plastic TQFP (Fine pitch) (12 × 12)

BLOCK DIAGRAM

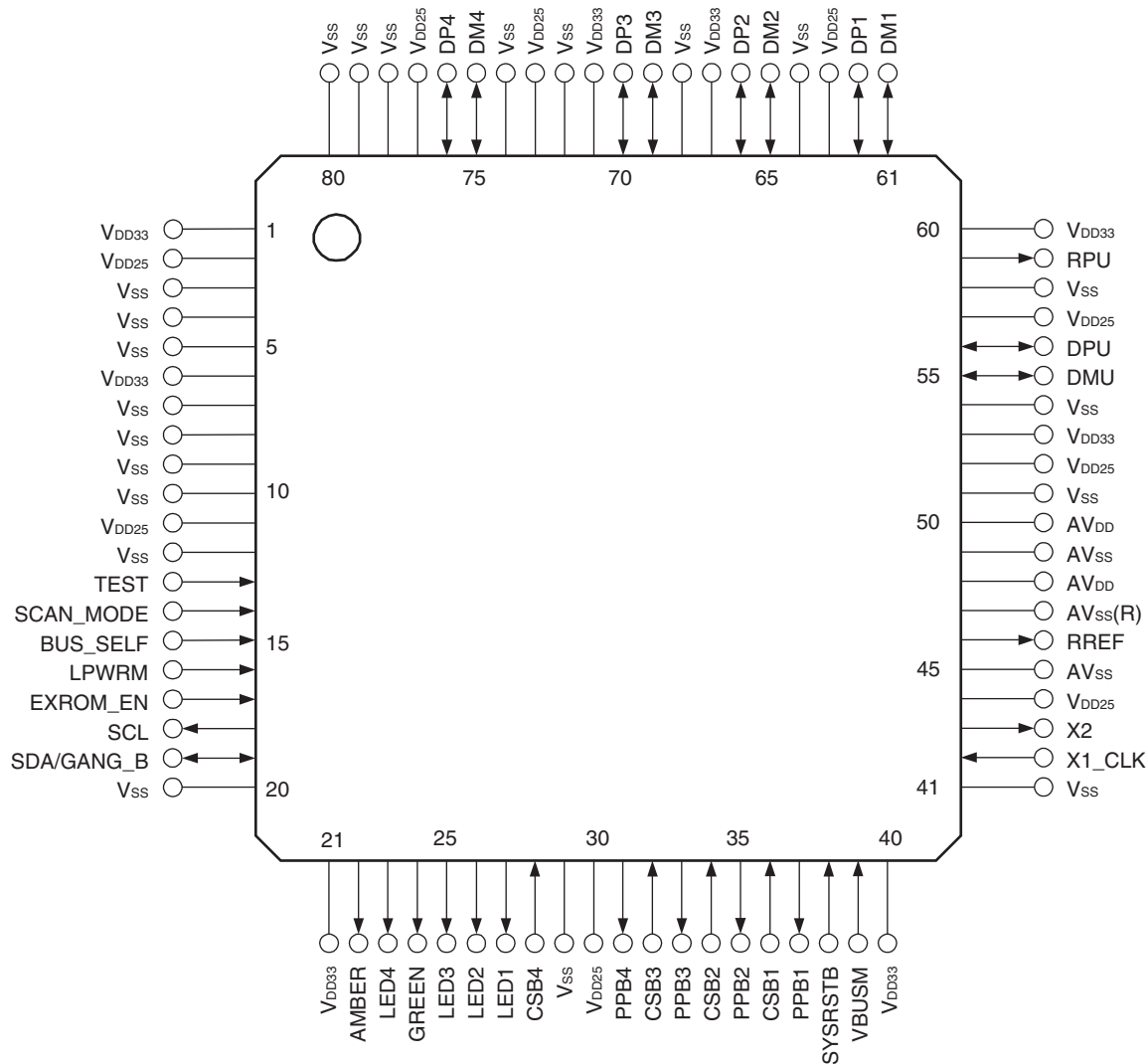


APLL	: Generates all clocks of Hub.
ALL_TT	: Translates the high-speed transactions (split transactions) for full/low-speed device to full/low-speed transactions. ALL_TT buffers the data transfer from either upstream or downstream direction. For OUT transaction, ALL_TT buffers data from upstream port and sends it out to the downstream facing ports after speed conversion from high-speed to full/low-speed. For IN transaction, ALL_TT buffers data from downstream ports and sends it out to the upstream facing ports after speed conversion from full/low-speed to high-speed.
CDR	: Data & clock recovery circuit
DPC	: Downstream Port Controller handles Port Reset, Enable, Disable, Suspend and Resume
DP(n)_PHY	: Downstream transceiver supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction
EP0	: Endpoint 0 controller
EP1	: Endpoint 1 controller
F_TIM (Frame Timer)	: Manages hub's synchronization by using micro-SOF which is received at upstream port, and generates SOF packet when full/low-speed device is attached to downstream facing port.
FS_REP	: Full/low-speed repeater is enabled when the μ PD720112 are worked at full-speed mode
OSB	: Oscillator Block
ROM I/F	: Interface block for external Serial ROM which contains user-defined descriptors
SERDES	: Serializer and Deserializer
SIE_2H	: Serial Interface Engine (SIE) controls USB2.0 and 1.1 protocol sequencer.
UP_PHY	: Upstream Transceiver supports high-speed (480 Mbps), full-speed (12 Mbps) transaction
UPC	: Upstream Port Controller handles Suspend and Resume

PIN CONFIGURATION (TOP VIEW)

- 80-pin plastic TQFP (Fine pitch) (12 × 12)

μPD720112GK-9EU



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{DD33}	21	V _{DD33}	41	V _{SS}	61	DM1
2	V _{DD25}	22	AMBER	42	X1_CLK	62	DP1
3	V _{SS}	23	LED4	43	X2	63	V _{DD25}
4	V _{SS}	24	GREEN	44	V _{DD25}	64	V _{SS}
5	V _{SS}	25	LED3	45	AV _{SS}	65	DM2
6	V _{DD33}	26	LED2	46	RREF	66	DP2
7	V _{SS}	27	LED1	47	AV _{SS} (R)	67	V _{DD33}
8	V _{SS}	28	CSB4	48	AV _{DD}	68	V _{SS}
9	V _{SS}	29	V _{SS}	49	AV _{SS}	69	DM3
10	V _{SS}	30	V _{DD25}	50	AV _{DD}	70	DP3
11	V _{DD25}	31	PPB4	51	V _{SS}	71	V _{DD33}
12	V _{SS}	32	CSB3	52	V _{DD25}	72	V _{SS}
13	TEST	33	PPB3	53	V _{DD33}	73	V _{DD25}
14	SCAN_MODE	34	CSB2	54	V _{SS}	74	V _{SS}
15	BUS_SELF	35	PPB2	55	DMU	75	DM4
16	LPWRM	36	CSB1	56	DPU	76	DP4
17	EXROM_EN	37	PPB1	57	V _{DD25}	77	V _{DD25}
18	SCL	38	SYSRSTB	58	V _{SS}	78	V _{SS}
19	SDA/GANG_B	39	VBUSM	59	RPU	79	V _{SS}
20	V _{SS}	40	V _{DD33}	60	V _{DD33}	80	V _{SS}

Remark AV_{SS}(R) should be used to connect RREF through 1 % precision reference resistor of 2.43 kΩ.

1. PIN INFORMATION

Pin Name	I/O	Buffer Type	Active Level	Function
X1_CLK	I	2.5 V input		Crystal oscillator in or clock input
X2	O	2.5 V output		Oscillator out
SYSRSTB	I	5 V tolerant Schmitt input	Low	Asynchronous chip reset
RPU	A (O)	USB pull-up control		External 1.5 kΩ pull-up resistor control
DP(4:1)	I/O	USB D+ signal I/O		USB's downstream facing port D+ signal
DM(4:1)	I/O	USB D− signal I/O		USB's downstream facing port D− signal
DPU	I/O	USB D+ signal I/O		USB's upstream facing port D+ signal
DMU	I/O	USB D− signal I/O		USB's upstream facing port D− signal
BUS_SELF	I	3.3 V Schmitt input		Power mode select
LPWRM	I	3.3 V Schmitt input		Local power monitor
RREF	A (O)	Analog		Reference resistor
CSB(4:1)	I	5 V tolerant input	Low	Port's over-current status input
PPB(4:1)	O	5 V tolerant N-ch open drain	Low	Port's power supply control output
VBUSM	I	5 V tolerant Schmitt input		V _{BUS} monitor
SCL	O	3.3 V output		External serial ROM clock out
SDA/GANG_B	I/O	3.3 V Schmitt I/O		External serial ROM data IO or power management mode select
EXROM_EN	I	3.3 V Schmitt input		External serial ROM input enable
AMBER	O	5 V tolerant output		Amber colored LED control output
GREEN	O	5 V tolerant output		Green colored LED control output
LED(4:1)	O	5 V tolerant output	Low	LED indicator output for downstream port status
TEST	I	3.3 V input		Test signal
SCAN_MODE	I	3.3 V input		Test signal
V _{DD33}				3.3 V V _{DD}
V _{DD25}				2.5 V V _{DD}
AV _{DD}				2.5 V V _{DD} for analog circuit
V _{SS}				V _{SS}
AV _{SS}				V _{SS} for analog circuit
AV _{SS} (R)				V _{SS} for reference resistor

Remark “5 V tolerant“ means that the buffer is 3 V buffer with 5 V tolerant circuit.

2. ELECTRICAL SPECIFICATIONS

2.1 Buffer List

- 2.5 V Oscillator interface
X1_CLK, X2
- 5 V Schmitt input buffer
SYSRSTB, CSB(4:1), VBUSM
- 3.3 V Schmitt input buffer
BUS_SELF, LPWRM
- 3.3 V input buffer
EXROM_EN, TEST, SCAN_MODE
- 3.3 V $I_{OL} = 3$ mA bi-directional Schmitt input buffer with input enable (OR-type)
SDA/GANG_B
- 3.3 V $I_{OL} = 3$ mA output buffer
SCL
- 5 V $I_{OL} = 12$ mA output buffer
AMBER, GREEN, LED2
- 5 V $I_{OL} = 12$ mA N-ch open drain buffer
PPB(4:1), LED4, LED3, LED1
- USB2.0 interface
RPU, DPU, DMU, DP(4:1), DM(4:1), RREF

Above, “5 V” refers to a 3 V buffer that is 5 V tolerant (has 5 V maximum voltage). Therefore, it is possible to have a 5 V connection for an external bus, but the output level will be only up to 3 V, which is the V_{DD33} voltage.

2.2 Terminology

Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V _{DD33} V _{DD25} A _{VDD}	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V _{DD} pin.
Input voltage	V _I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V _O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I _O	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when a current flow out of or into an output pin.
Operating temperature	T _A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T _{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device.

Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V _{DD33} V _{DD25} A _{VDD}	Indicates the voltage range for normal logic operations occur when V _{SS} = 0 V.
High-level input voltage	V _{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the "MIN." value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V _{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the "MAX." value is applied, the input voltage is guaranteed as low level voltage.
Hysteresis voltage	V _H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rise time	t _{ri}	Indicates allowable input rise time to input pins. Input rise time is transition time from 0.1 × V _{DD} to 0.9 × V _{DD} .
Input fall time	t _{fi}	Indicates allowable input fall time to input pins. Input fall time is transition time from 0.9 × V _{DD} to 0.1 × V _{DD} .

Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pin is shorted (to GND pins) when output is at high-level.
Input leakage current	I_I	Indicates the current that flows when the input voltage is supplied to the input pin.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that flows from the output pins when the rated high-level output voltage is being applied.

2.3 Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD33}		−0.5 to +4.6	V
	V_{DD25}		−0.5 to +3.6	V
	AV_{DD}		−0.5 to +3.6	V
Input/output voltage	V_I/V_O			
2.5V input/output voltage		$2.3\text{ V} \leq V_{DD25} \leq 2.7\text{ V}$ $V_I/V_O < V_{DD25} + 0.9\text{ V}$	−0.5 to +3.6	V
3.3 V input/output voltage		$3.0\text{ V} \leq V_{DD33} \leq 3.6\text{ V}$ $V_I/V_O < V_{DD33} + 1.0\text{ V}$	−0.5 to +4.6	V
5 V input/out voltage		$3.0\text{ V} \leq V_{DD33} \leq 3.6\text{ V}$ $V_I/V_O < V_{DD33} + 3.0\text{ V}$	−0.5 to +6.6	V
Output current	I_O	$I_{OL} = 3\text{ mA}$	10	mA
		$I_{OL} = 6\text{ mA}$	20	mA
		$I_{OL} = 12\text{ mA}$	40	mA
Operating temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Recommended Operating Ranges

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating voltage	V _{DD33}	3.3 V for V _{DD33} pins	3.14	3.30	3.46	V
	V _{DD25}	2.5 V for V _{DD25} pins	2.3	2.5	2.7	V
	AV _{DD}	2.5 V for AV _{DD} pins	2.3	2.5	2.7	V
High-level input voltage	V _{IH}					
2.5 V High-level input voltage			1.7		V _{DD25}	
3.3 V High-level input voltage			2.0		V _{DD33}	V
5.0 V High-level input voltage			2.0		5.5	V
Low-level input voltage	V _{IL}					
2.5 V Low-level input voltage			0		0.7	
3.3 V Low-level input voltage			0		0.8	V
5.0 V Low-level input voltage			0		0.8	V
Hysteresis voltage	V _H					
5 V Hysteresis voltage			0.3		1.5	V
3.3 V Hysteresis voltage			0.2		1.0	V
Input rise time for SYSRSTB	t _{rst}				10	ms
Input rise time	t _{ri}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms
Input fall time	t _{fi}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms

Two power supply rails limitation.

The μPD720112 has two power supply rails (2.5 V, 3.3 V). The μPD720112 requires that V_{DD25} should be stable before V_{DD33} becomes stable. The system will require the time when power supply rail is stable at V_{DD} level. And, there will be difference between the time of V_{DD25} and V_{DD33}. At any case, the system must ensure that the absolute maximum ratings for V_I / V_O are not exceeded. System reset signaling should be asserted more than specified time after both V_{DD25} and V_{DD33} are stable.

DC Characteristics

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Off-state output leakage current	I_{OZ}	$V_O = V_{DD33}, V_{DD25} \text{ or } V_{SS}$		± 10	μA
Output short circuit current	I_{OS} ^{Note}			-250	mA
Low-level output current	I_{OL}				
3.3 V low-level output current		$V_{OL} = 0.4 \text{ V}$	3		mA
3.3 V low-level output current		$V_{OL} = 0.4 \text{ V}$	6		mA
5.0 V low-level output current		$V_{OL} = 0.4 \text{ V}$	12		mA
High-level output current	I_{OH}				
3.3 V high-level output current		$V_{OH} = 2.4 \text{ V}$	-3		mA
3.3 V high-level output current		$V_{OH} = 2.4 \text{ V}$	-6		mA
5.0 V high-level output current		$V_{OH} = 2.4 \text{ V}$	-2		mA
Input leakage current	I_I				
3.3 V buffer		$V_I = V_{DD} \text{ or } V_{SS}$		± 10	μA
5.0 V buffer		$V_I = V_{DD} \text{ or } V_{SS}$		± 10	μA

Note The output short circuit time is measured at one second or less and is tested with only one pin on the LSI.

USB Interface Block

Parameter	Symbol	Conditions	MIN	MAX	Unit
Output pin impedance	Z _{HSDRV}	Includes R _S resistor	40.5	49.5	Ω
Bus pull-up resistor on upstream facing port	R _{PU}		1.425	1.575	kΩ
Bus pull-up resistor on downstream facing port	R _{PD}		14.25	15.75	kΩ
Termination voltage for upstream facing port pullup (full-speed)	V _{TERM}		3.0	3.6	V
Input Levels for Low-/full-speed:					
High-level input voltage (drive)	V _{IH}		2.0		V
High-level input voltage (floating)	V _{IHZ}		2.7	3.6	V
Low-level input voltage	V _{IL}			0.8	V
Differential input sensitivity	V _{DI}	(D+) – (D–)	0.2		V
Differential common mode range	V _{CM}	Includes V _{DI} range	0.8	2.5	V
Output Levels for Low-/full-speed:					
High-level output voltage	V _{OH}	R _L of 14.25 kΩ to GND	2.8	3.6	V
Low-level output voltage	V _{OL}	R _L of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V _{OSE1}		0.8		V
Output signal crossover point voltage	V _{CRS}		1.3	2.0	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	V _{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal)	V _{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range	V _{HSCM}		–50	+500	mV
High-speed differential input signaling levels	See Figure 2-4.				
Output Levels for High-speed:					
High-speed idle state	V _{HSOI}		–10.0	+10	mV
High-speed data signaling high	V _{HSOH}		360	440	mV
High-speed data signaling low	V _{HSOL}		–10.0	+10	mV
Chirp J level (different signal)	V _{CHIRPJ}		700	1100	mV
Chirp K level (different signal)	V _{CHIRPK}		–900	–500	mV

Figure 2-1. Differential Input Sensitivity Range for Low-/full-speed

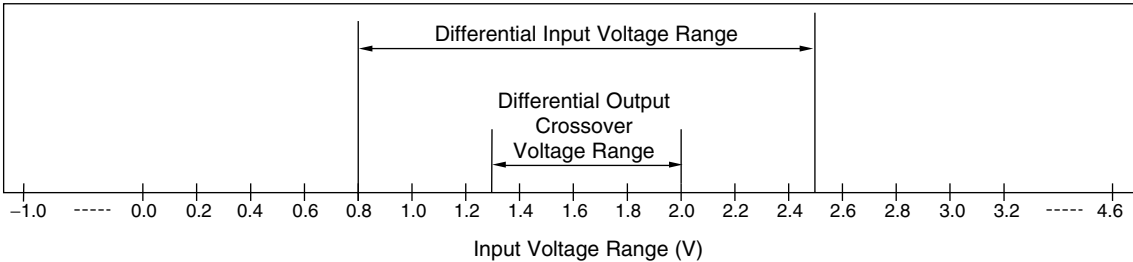


Figure 2-2. Full-speed Buffer V_{OH}/I_{OH} Characteristics for High-speed Capable Transceiver

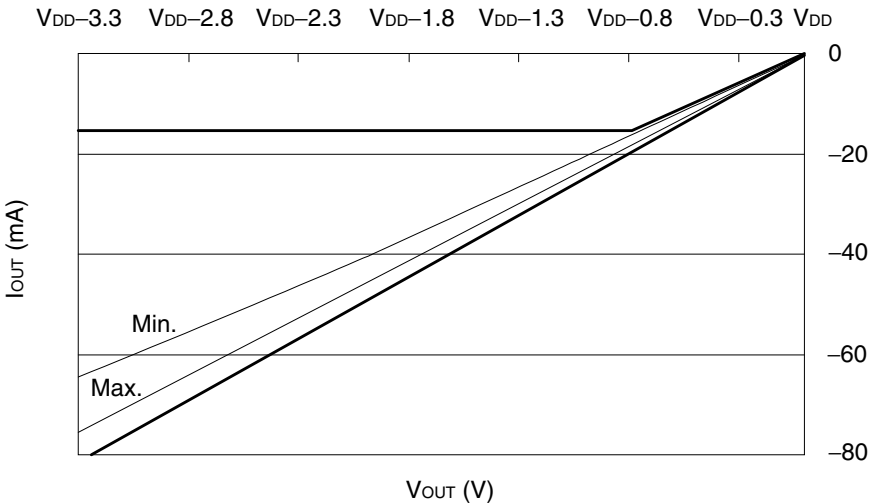


Figure 2-3. Full-speed Buffer V_{OL}/I_{OL} Characteristics for High-speed Capable Transceiver

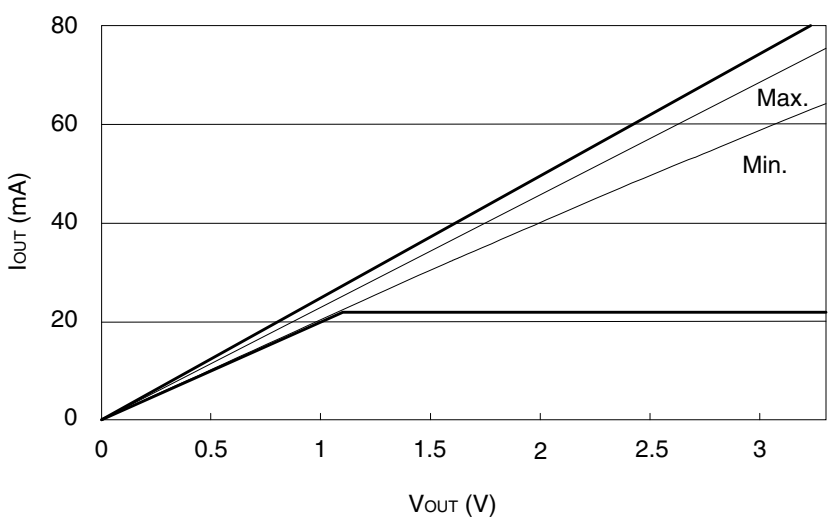


Figure 2-4. Receiver Sensitivity for Transceiver at DP/DM

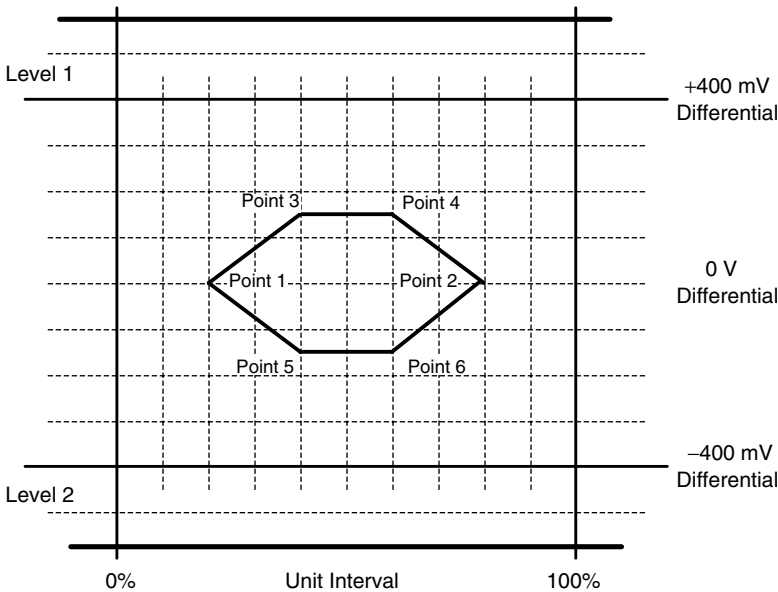
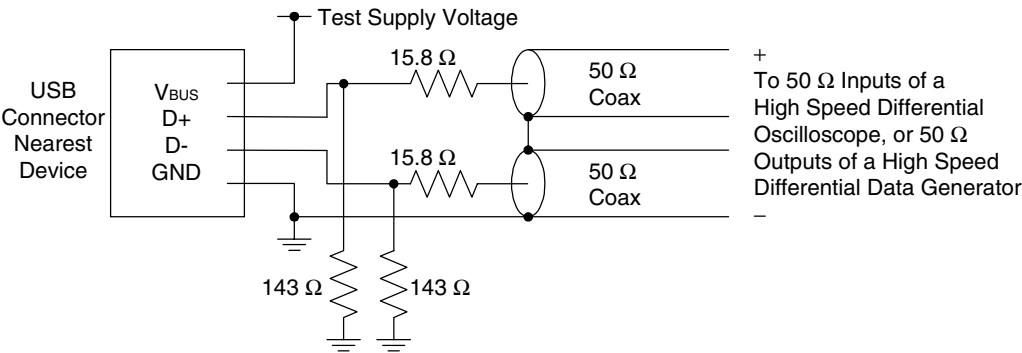


Figure 2-5. Receiver Measurement Fixtures



Power Consumption

Parameter	Symbol	Condition	TYP.	Unit
Power Consumption	P _{W-0}	The power consumption under the state without suspend. All the ports do not connect to any function. ^{Note}		
		Hub controller is operating at full-speed mode.	43	mA (2.5 V)
			2.4	mA (3.3 V)
		Hub controller is operating at high-speed mode.	83	mA (2.5 V)
	P _{W-2}		23	mA (3.3 V)
		The power consumption under the state without suspend. The number of active ports is 2.		
		Hub controller is operating at full-speed mode.	43	mA (2.5 V)
			6.0	mA (3.3 V)
	P _{W-3}		108	mA (2.5 V)
		Hub controller is operating at high-speed mode.	49	mA (3.3 V)
		The power consumption under the state without suspend. The number of active ports is 3.		
		Hub controller is operating at full-speed mode.	43	mA (2.5 V)
	P _{W-4}		7.7	mA (3.3 V)
		Hub controller is operating at high-speed mode.	118	mA (2.5 V)
			62	mA (3.3 V)
		The power consumption under the state without suspend. The number of active ports is 4.		
	P _{W-S}		43	mA (2.5 V)
		Hub controller is operating at full-speed mode.	9.3	mA (3.3 V)
		Hub controller is operating at high-speed mode.	127	mA (2.5 V)
			75	mA (3.3 V)
	P _{W-S}	The power consumption under suspend state.	0.66	mA (2.5 V)
		The internal clock is stopped.	0.50	mA (3.3 V)

Note When any device is not connected to all the ports, the power consumption does not depend on the number of active ports.

System Clock Ratings

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock frequency	f _{CLK}	X'tal	−500 ppm	30	+500 ppm	MHz
		Oscillator block	−500 ppm	30	+500 ppm	MHz
Clock Duty cycle	t _{DUTY}		40	50	60	%

Remarks 1. Mandatory accuracy of clock frequency is ± 100 ppm.

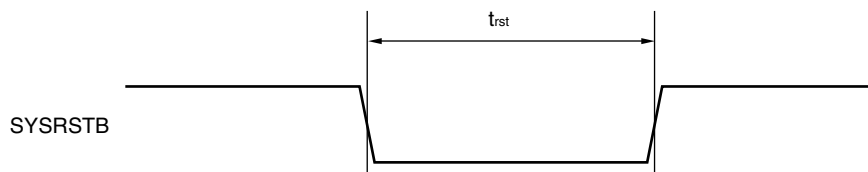
2. Required accuracy of X'tal or oscillator block is including initial frequency accuracy, the spread of X'tal capacitor loading, supply voltage, temperature, and aging, etc.

AC Characteristics (V_{DD} = 3.14 to 3.46 V, T_A = 0 to +70°C)

System Reset Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Reset active time (Figure 2-6)	t _{rst}		5		μs

Figure 2-6. System Reset Timing



Over-current Response Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Over-current response time from CSB low to PPB high (Figure 2-7)	t_{oc}		500		625	μs

Figure 2-7. Over-current Response Timing

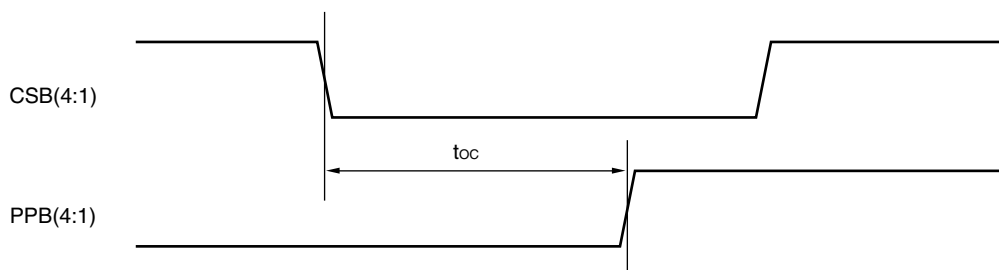
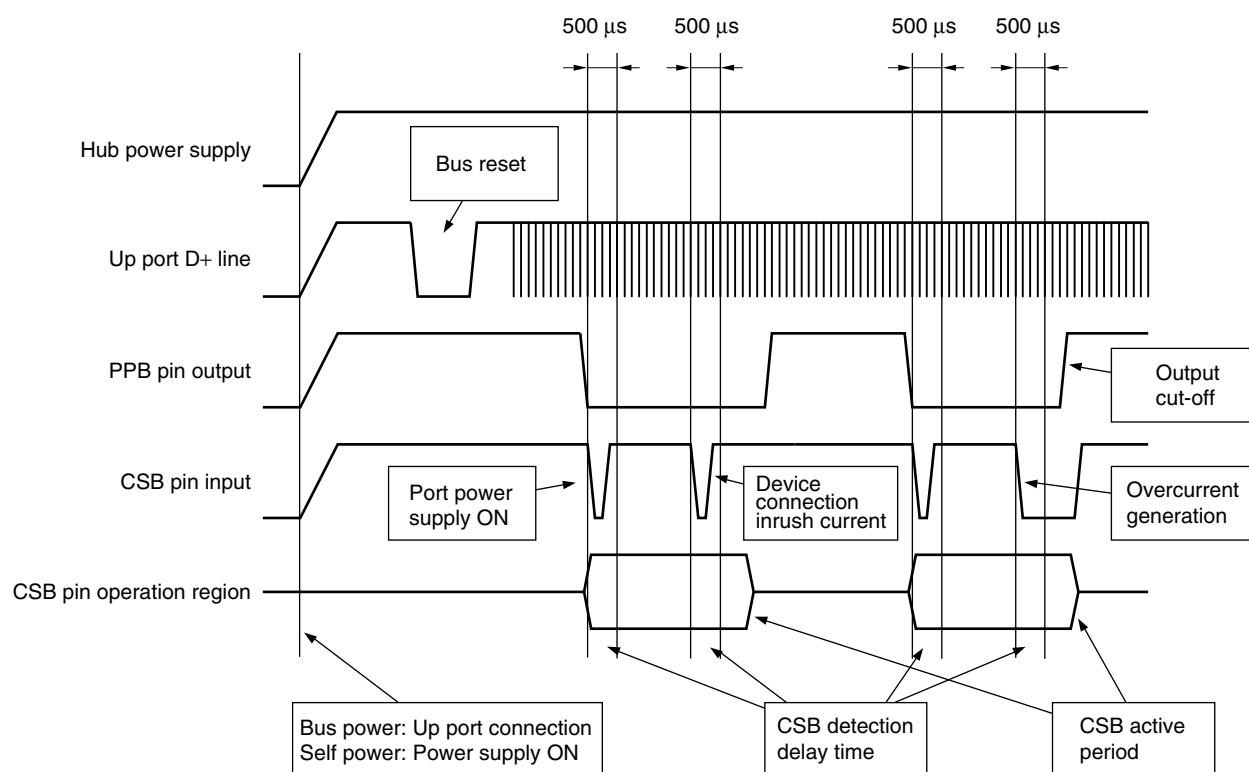


Figure 2-8. CSB/PPB Timing



Remark The active period of the CSB pin is in effect only when the PPB pin is ON.
There is a delay time of approximately 500 μs duration at the CSB pin.

External Serial ROM Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock frequency	f_{SCL}			94.6	100	kHz
Clock pulse width low	t_{LOW}		4700			ns
Clock pulse width high	t_{HIGH}		4000			ns
Clock low to data out valid	t_{AA}		100		3500	ns
Time the bus must be free before a new transmission can start	t_{BUF}		4700			ns
Start hold time	$t_{HD.STA}$		4000			ns
Start setup time	$t_{SU.STA}$		4700			ns
Data in hold time	$t_{HD.DTA}$		0			ns
Data in setup time	$t_{SU.DTA}$		250			ns
Stop setup time	$t_{SU.STO}$		4700			ns
Data out hold time	t_{DH}		300			ns
Write cycle time	t_{WR}				15	ms

Figure 2-9. External Serial ROM Bus Timing

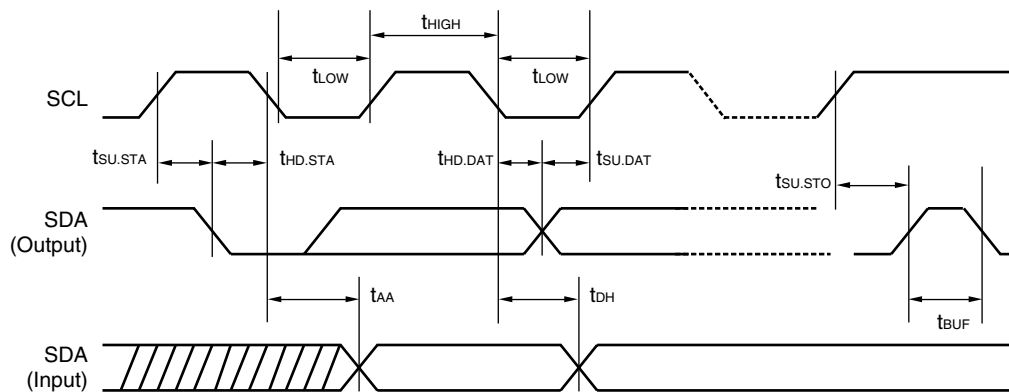
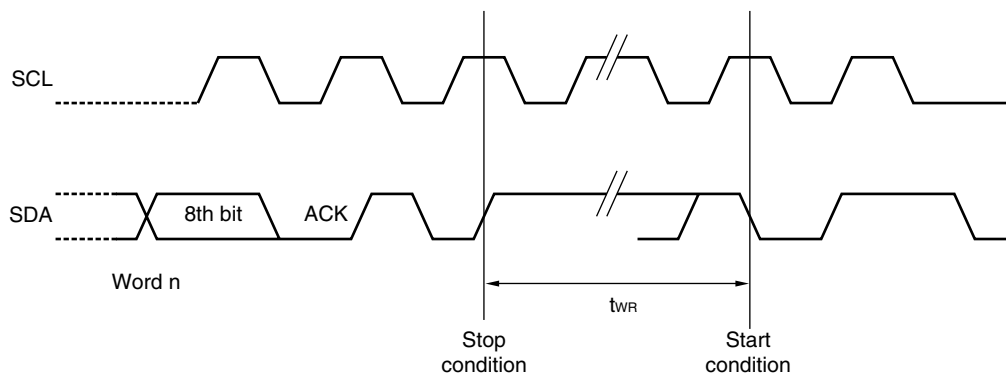


Figure 2-10. External Serial ROM Write Cycle Timing



USB Interface Block

(1/4)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Low-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{LR}	$C_L = 200 \text{ pF to } 600 \text{ pF}$	75	300	ns
Fall time (90% to 10%)	t_{LF}	$C_L = 200 \text{ pF to } 600 \text{ pF}$	75	300	ns
Differential rise and fall time matching	t_{LRFM}	(t_{LR}/t_{LF}) ^{Note}	80	125	%
Low-speed data rate	$t_{LDRATHS}$	Average bit rate	1.49925	1.50075	Mbps
Downstream facing port source jitter total (including frequency tolerance) (Figure 2-15):					
To next transition	t_{DDJ1}		-25	+25	ns
For paired transitions	t_{DDJ2}		-14	+14	ns
Downstream facing port differential receiver jitter total (including frequency tolerance) (Figure 2-17):					
To next transition	t_{UJR1}		-152	+152	ns
For paired transitions	t_{UJR2}		-200	+200	ns
Source SE0 interval of EOP (Figure 2-16)	t_{LEOPT}		1.25	1.5	μs
Receiver SE0 interval of EOP (Figure 2-16)	t_{LEOPR}		670		ns
Width of SE0 interval during differential transition	t_{LST}			210	ns
Hub differential data delay (Figure 2-13)	t_{LHDD}			300	ns
Hub differential driver jitter (including cable) (Figure 2-13):					
Downstream facing port					
To next transition	t_{LDHJ1}		-45	+45	ns
For paired transitions	t_{LDHJ2}		-15	+15	ns
Upstream facing port					
To next transition	t_{LUHJ1}		-45	+45	ns
For paired transitions	t_{LUHJ2}		-45	+45	ns
Data bit width distortion after SOP (Figure 2-13)	t_{LSOP}		-60	+60	ns
Hub EOP delay relative to t_{HDD} (Figure 2-14)	t_{LEOPD}		0	200	ns
Hub EOP output width skew (Figure 2-14)	t_{LHESK}		-300	+300	ns
Full-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{FR}	$C_L = 50 \text{ pF},$ $R_S = 36 \Omega$	4	20	ns
Fall time (90% to 10%)	t_{FF}	$C_L = 50 \text{ pF},$ $R_S = 36 \Omega$	4	20	ns
Differential rise and fall time matching	t_{FRFM}	(t_{FR}/t_{FF})	90	111.11	%
Full-speed data rate	$t_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t_{FRAME}		0.9995	1.0005	ms

Note Excluding the first transition from the Idle state.

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Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Full-speed Electrical Characteristics (Continued)					
Consecutive frame interval jitter	t _{RFI}	No clock adjustment		42	ns
Source jitter total (including frequency tolerance) (Figure 2-15):		Note			
To next transition	t _{DJ1}		−3.5	+3.5	ns
For paired transitions	t _{DJ2}		−4.0	+4.0	ns
Source jitter for differential transition to SE0 transition (Figure 2-16)	t _{FDEOP}		−2	+5	ns
Receiver jitter (Figure 2-17):					
To Next Transition	t _{JR1}		−18.5	+18.5	ns
For Paired Transitions	t _{JR2}		−9	+9	ns
Source SE0 interval of EOP (Figure 2-16)	t _{FEOPT}		160	175	ns
Receiver SE0 interval of EOP (Figure 2-16)	t _{FEOPR}		82		ns
Width of SE0 interval during differential transition	t _{FST}			14	ns
Hub differential data delay (Figure 2-13)					
(with cable)	t _{HDD1}			70	ns
(without cable)	t _{HDD2}			44	ns
Hub differential driver jitter (including cable) (Figure 2-13):					
To next transition	t _{HDJ1}		−3	+3	ns
For paired transitions	t _{HDJ2}		−1	+1	ns
Data bit width distortion after SOP (Figure 2-13)	t _{FSOP}		−5	+5	ns
Hub EOP delay relative to t _{HDD} (Figure 2-14)	t _{FEOPD}		0	15	ns
Hub EOP output width skew (Figure 2-14)	t _{FHESK}		−15	+15	ns
High-speed Electrical Characteristics					
Rise time (10% to 90%)	t _{HSR}		500		ps
Fall time (90% to 10%)	t _{HSF}		500		ps
Driver waveform	See Figure 2-11.				
High-speed data rate	t _{HSDRAT}		479.760	480.240	Mbps
Microframe interval	t _{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	t _{HSRFI}			4 high-speed	Bit times
Data source jitter	See Figure 2-11.				
Receiver jitter tolerance	See Figure 2-4.				
Hub data delay (without cable)	t _{SHDD}			36 high-speed+4 ns	Bit times
Hub data jitter	See Figure 2-4, Figure 2-11.				
Hub delay variation range	t _{SHDVB}			5 high-speed	Bit times

Note Excluding the first transition from the Idle state.

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Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Hub Event Timings					
Time to detect a downstream facing port connect event (Figure 2-19): Awake hub Suspended hub	tDCNN		2.5 2.5	2000 12000	μ s μ s
Time to detect a disconnect event at a hub's downstream facing port (Figure 2-18)	tDDIS		2.0	2.5	μ s
Duration of driving resume to a downstream port (only from a controlling hub)	tDRSMON		20		ms
Time from detecting downstream resume to rebroadcast	tURSM			1.0	ms
Duration of driving reset to a downstream facing port (Figure 2-20)	tDRST	Only for a SetPortFeature (PORT_RESET) request	10	20	ms
Time to detect a long K from upstream	tURLK		2.5	100	μ s
Time to detect a long SE0 from upstream	tURLSE0		2.5	10000	μ s
Duration of repeating SE0 upstream (for low-/full-speed repeater)	tURPSE0			23	FS Bit times
Inter-packet delay (for high-speed) of packets traveling in same direction	tHSIPDSD		88		Bit times
Inter-packet delay (for high-speed) of packets traveling in opposite direction	tHSIPDOD		8		Bit times
Inter-packet delay for device/root hub response with detachable cable for high-speed	tHSRSPID1			192	Bit times
Time of which a Chirp J or Chirp K must be continuously detected (filtered) by hub or device during Reset handshake	tFILT		2.5		μ s
Time after end of device Chirp K by which hub must start driving first Chirp K in the hub's chirp sequence	tWTDCH			100	μ s
Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream by hub during reset	tDCHBIT		40	60	μ s
Time before end of reset by which a hub must end its downstream chirp sequence	tDCHSE0		100	500	μ s
Time from internal power good to device pulling D+ beyond V _{IHZ} (Figure 2-20)	tSIGATT			100	ms
Debounce interval provided by USB system software after attach (Figure 2-20)	tATTDB			100	ms
Maximum duration of suspend averaging interval	tSUSAVGI			1	s
Period of idle bus before device can initiate resume	tWTRSM		5		ms
Duration of driving resume upstream	tDRSMUP		1	15	ms

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Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Hub Event Timings (Continued)					
Resume recovery time	t _{RSRMCY}	Remote-wakeup is enabled	10		ms
Time to detect a reset from upstream for non high-speed capable devices	t _{DETRST}		2.5	10000	μs
Reset recovery time (Figure 2-20)	t _{RSTRCY}			10	ms
Inter-packet delay for full-speed	t _{IPD}		2		Bit times
Inter-packet delay for device response with detachable cable for full-speed	t _{RSPIPD1}			6.5	Bit times
SetAddress() completion time	t _{DSETADDR}			50	ms
Time to complete standard request with no data	t _{DRQCMLTND}			50	ms
Time to deliver first and subsequent (except last) data for standard request	t _{DRETDATA1}			500	ms
Time to deliver last data for standard request	t _{DRETDATAN}			50	ms
Time for which a suspended hub will see a continuous SE0 on upstream before beginning the high-speed detection handshake	t _{FILTSE0}		2.5		μs
Time a hub operating in non-suspended full-speed will wait after start of SE0 on upstream before beginning the high-speed detection handshake	t _{WTRSTFS}		2.5	3000	ms
Time a hub operating in high-speed will wait after start of SE0 on upstream before reverting to full-speed	t _{WTREV}		3.0	3.125	ms
Time a hub will wait after reverting to full-speed before sampling the bus state on upstream and beginning the high-speed will wait after start of SE0 on upstream before reverting to full-speed	t _{WTRSTHS}		100	875	ms
Minimum duration of a Chirp K on upstream from a hub within the reset protocol	t _{UCH}		1.0		ms
Time after start of SE0 on upstream by which a hub will complete its Chirp K within the reset protocol	t _{UCHEND}			7.0	ms
Time between detection of downstream chip and entering high-speed state	t _{WTHS}			500	μs
Time after end of upstream Chirp at which hub reverts to full-speed default state if no downstream Chirp is detected	t _{WTFS}		1.0	2.5	ms

Figure 2-11. Transmit Waveform for Transceiver at DP/DM

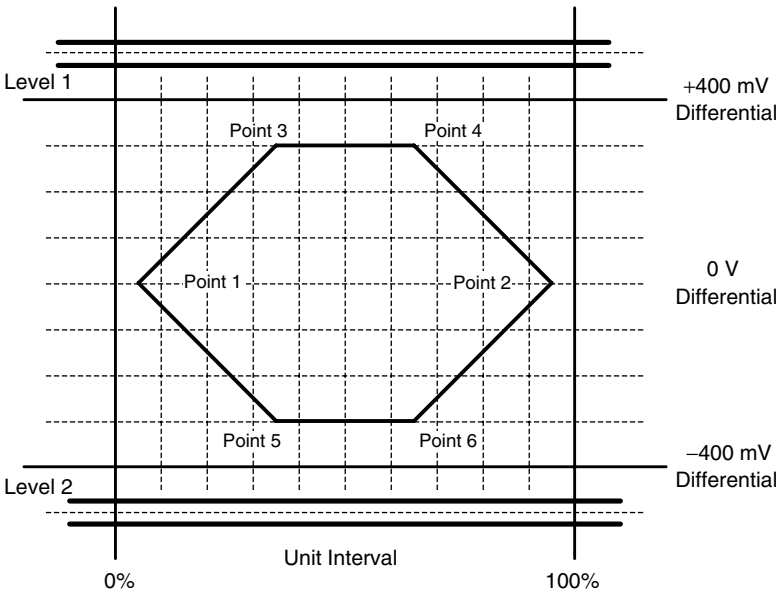
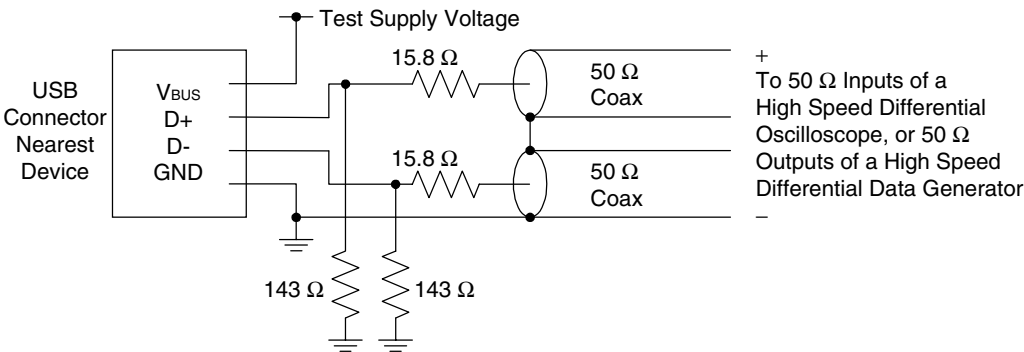
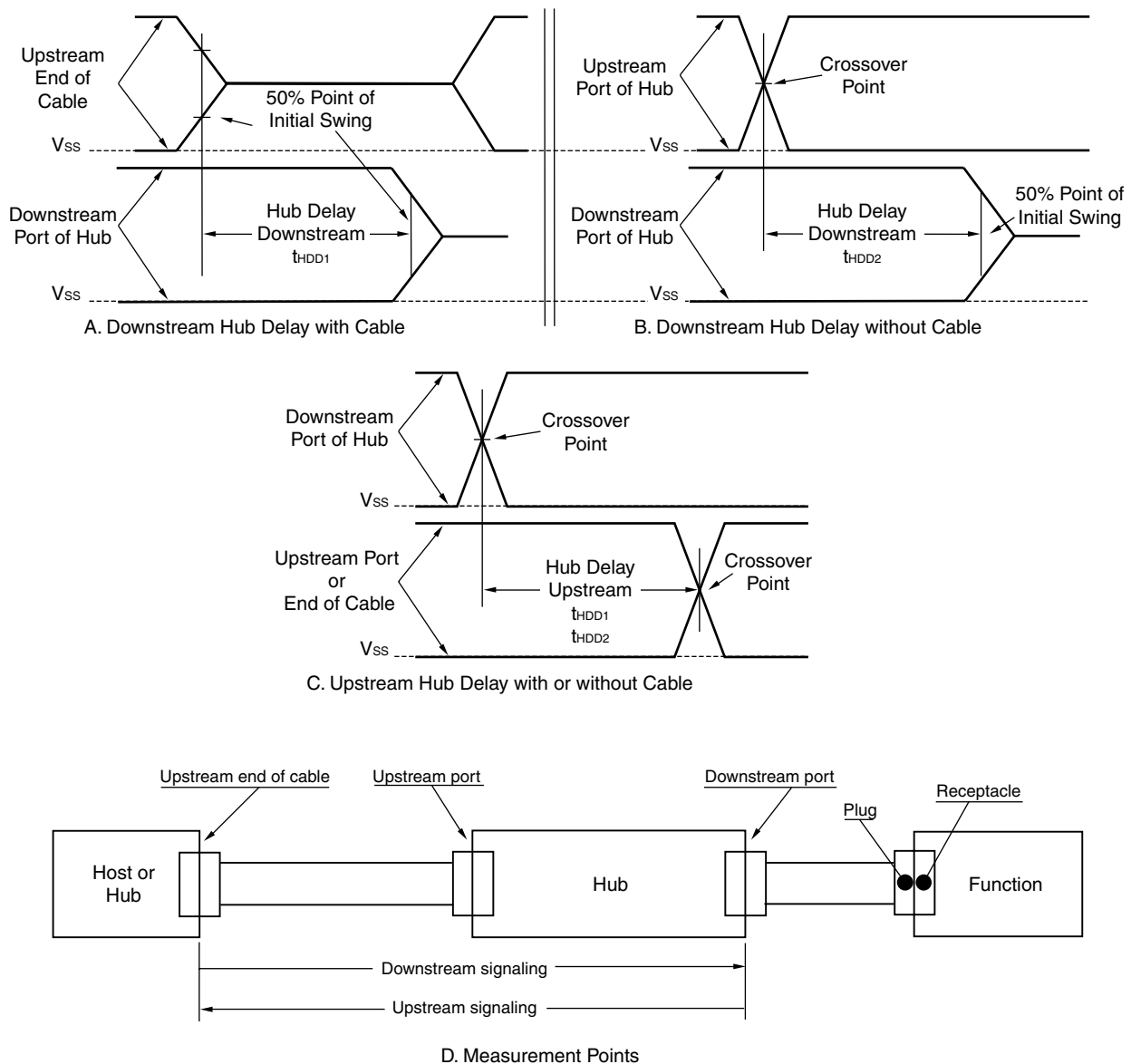


Figure 2-12. Transmitter Measurement Fixtures



Timing Diagram

Figure 2-13. Hub Differential Delay, Differential Jitter, and SOP Distortion



Hub Differential Jitter:

$$t_{HDJ1} = t_{HDDx}(J) - t_{HDDx}(K) \text{ or } t_{HDDx}(K) - t_{HDDx}(J) \quad \text{Consecutive Transitions}$$

$$t_{HDJ2} = t_{HDDx}(J) - t_{HDDx}(J) \text{ or } t_{HDDx}(K) - t_{HDDx}(K) \quad \text{Paired Transitions}$$

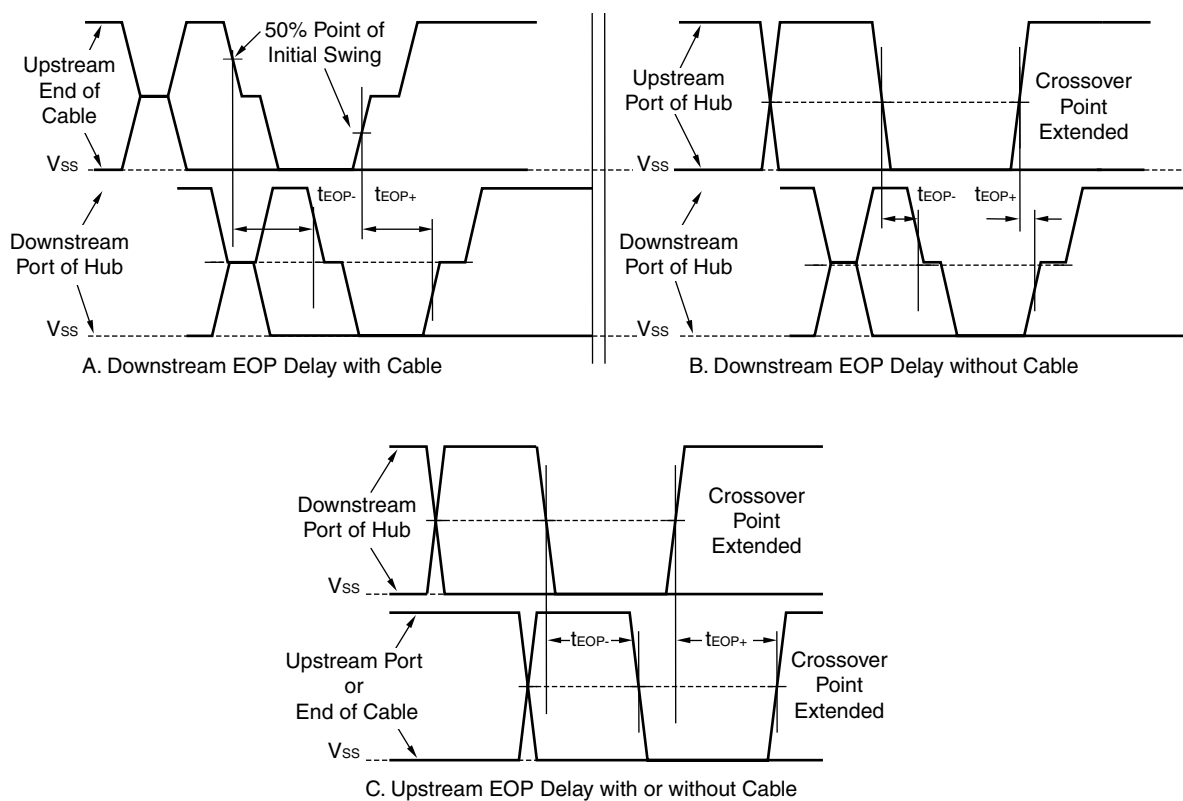
Bit after SOP Width Distortion (same as data jitter for SOP and next J transition):

$$t_{FSOP} = t_{HDDx}(\text{next J}) - t_{HDDx}(\text{SOP})$$

Low-speed timings are determined in the same way for:

$$t_{LHDD}, t_{LDHJ1}, t_{LDJH2}, t_{LUHJ1}, t_{LUJH2}, \text{ and } t_{LSOP}$$

Figure 2-14. Hub EOP Delay and EOP Skew

**EOP Delay:**

$$t_{FEOPD} = t_{EOPy} - t_{HDDx}$$

(t_{EOPy} means that this equation applies to t_{EOP-} and t_{EOP+})

EOP Skew:

$$t_{FHESK} = t_{EOP+} - t_{EOP-}$$

Low-speed timings are determined in the same way for:

t_{LEOPD} and t_{LHESK}

Figure 2-15. USB Differential Data Jitter for Low-/full-speed

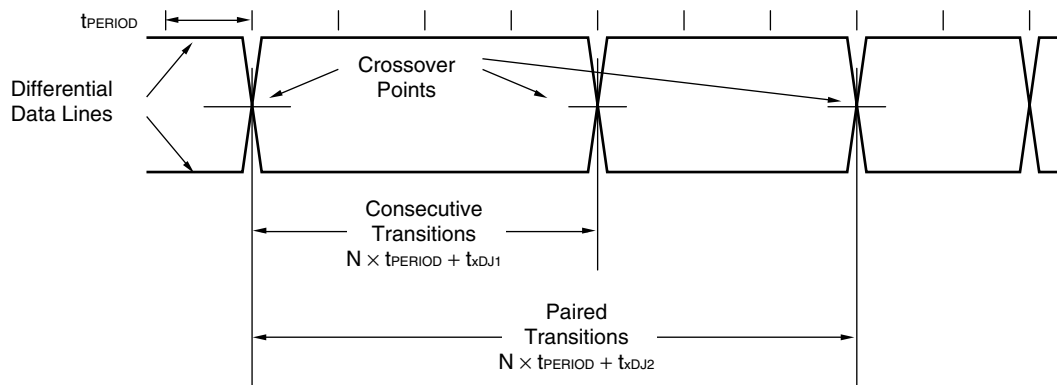


Figure 2-16. USB Differential-to-EOP Transition Skew and EOP Width for Low-/full-speed

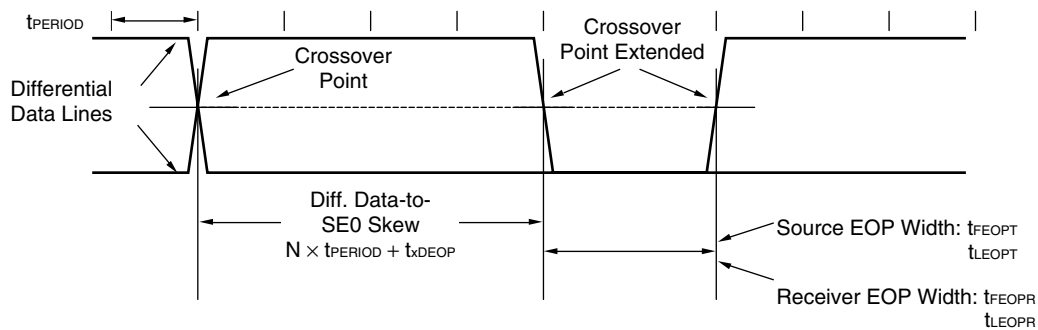


Figure 2-17. USB Receiver Jitter Tolerance for Low-/full-speed

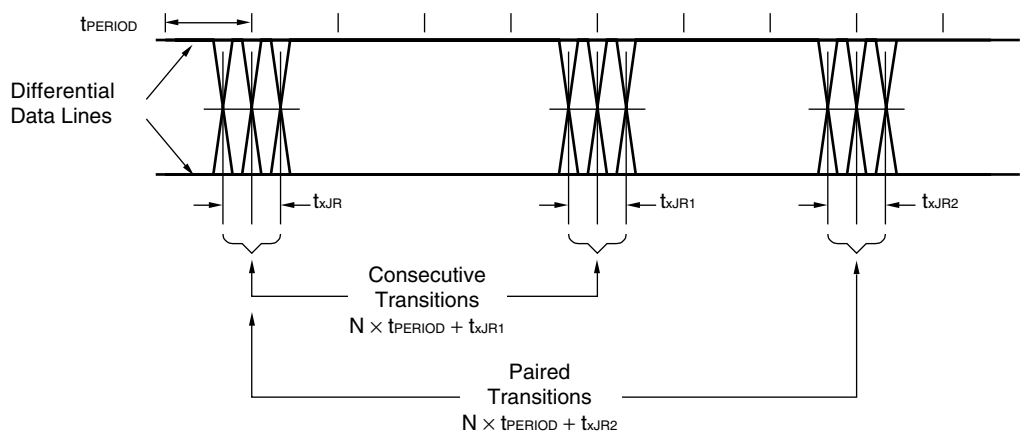


Figure 2-18. Low-/full-speed Disconnect Detection

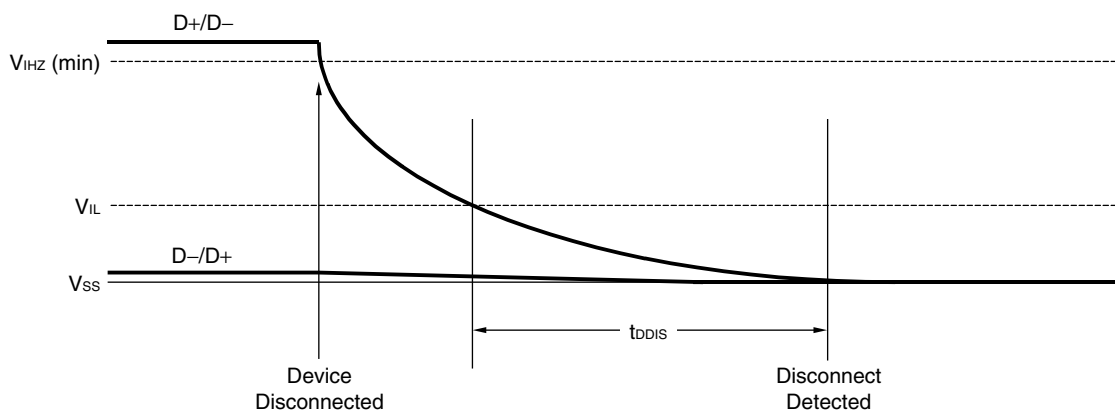


Figure 2-19. Full-/high-speed Device Connect Detection

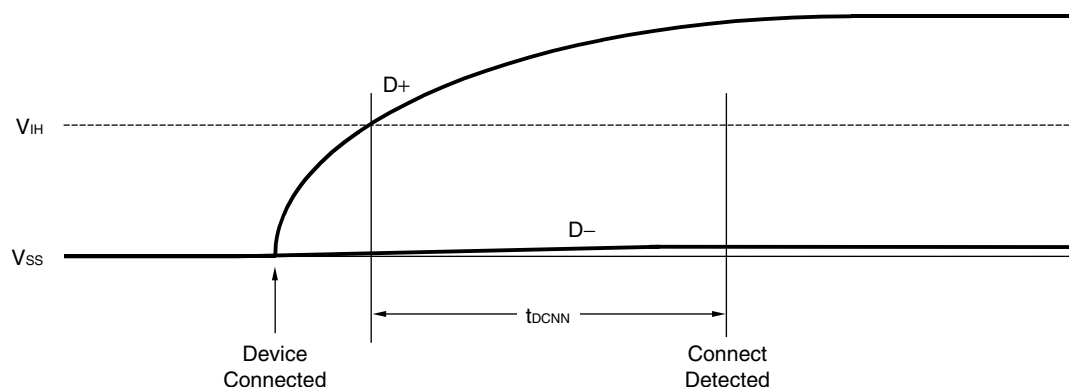
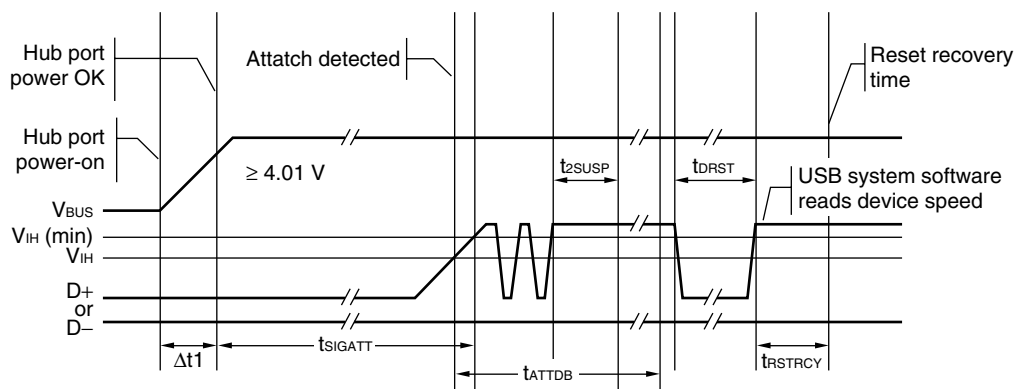
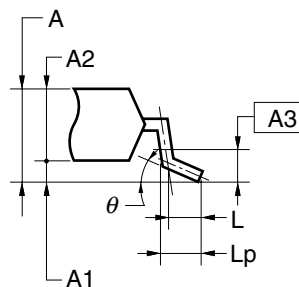
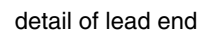


Figure 2-20. Power-on and Connection Events Timing



80-PIN PLASTIC TQFP (FINE PITCH) (12x12)



ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
A2	1.00
HD	14.00±0.20
HE	14.00±0.20
A	1.10±0.10
A1	0.10±0.05
A3	0.25
Lp	0.60±0.15
b	0.22±0.05
c	0.17 ^{+0.03} _{-0.07}
θ	3° ^{+4°} _{-3°}
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25
L	0.50
L1	1.00±0.20

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

4. RECOMMENDED SOLDERING CONDITIONS

The μPD720112 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

μPD720112GK-9EU: 80-pin plastic TQFP (Fine pitch) (12 × 12)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less Exposure limit: 3 days ^{Note} (after that, prebake at 125°C for 10 hours)	IR35-103-3
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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