FAIRCHILD SEMICONDUCTOR®

February 2007

FAN7385
Dual-Channel High-Side Gate-Drive IC

Features

- Floating Channel for Bootstrap Operation to +600V
- Typically 350mA/650mA Sourcing/Sinking Current Driving Capability
- Extended Allowable Negative V_S Swing to -9.8V for Signal Propagation at V_{DD}=V_{BS}=15V
- High-Side Output In-Phase of Input Signal
- V_{DD} & V_{BS} Supply Range from 10V to 20V
- 3.3V and 5V Input Logic Compatible
- Built-in Common Mode dv/dt Noise Canceling Circuit
- Built-in UVLO Functions for Both Channels

Applications

- Normal Half-Bridge and Full-Bridge Driver
- PDP Energy Recovery Switch Control Driver
- Switching Mode Power Supply

Description

The FAN7385 is a monolithic high side gate drive IC designed for high voltage, high speed driving MOSFETs and IGBTs operating up to +600V.

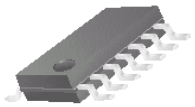
Fairchild's high-voltage process and common-mode noise canceling technique provide stable operation of high-side drivers under high-dv/dt noise circumstances.

An advanced level-shift circuit allows high-side gate driver operation up to V_S = -9.8V (typical) for V_{BS} = 15V.

The UVLO circuits prevent malfunction when V_{BS1} and V_{BS2} are lower than the specified threshold voltage.

Output drivers typically source/sink 350mA/650mA, respectively, which is suitable for dual high-side switches and half-bridge inverters.

14-SOP



Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packing Method
FAN7385M(1)	14-SOP	Yes	-40°C ~ 125°C	Tube
FAN7385MX(1)				Tape & Reel

Note:

1. These devices passed wave soldering test by JESD22A-111.

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Typical Application Diagrams

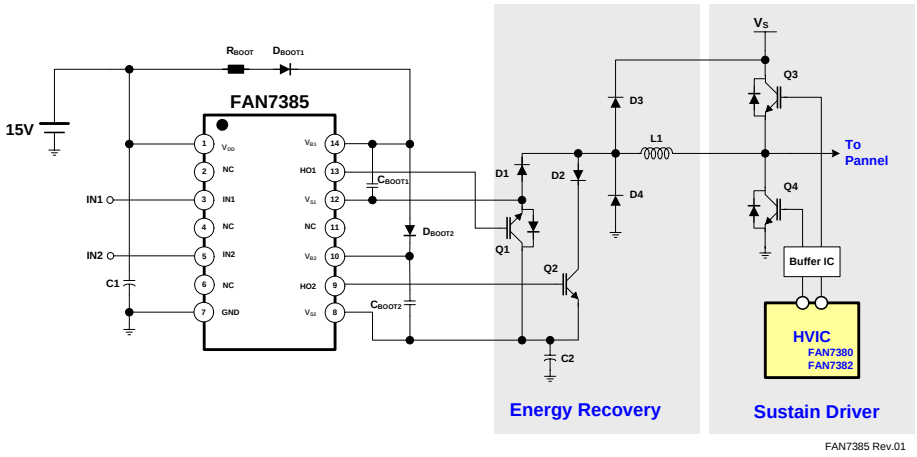


Figure 1. Floated Bidirectional Switch Control for PDP application

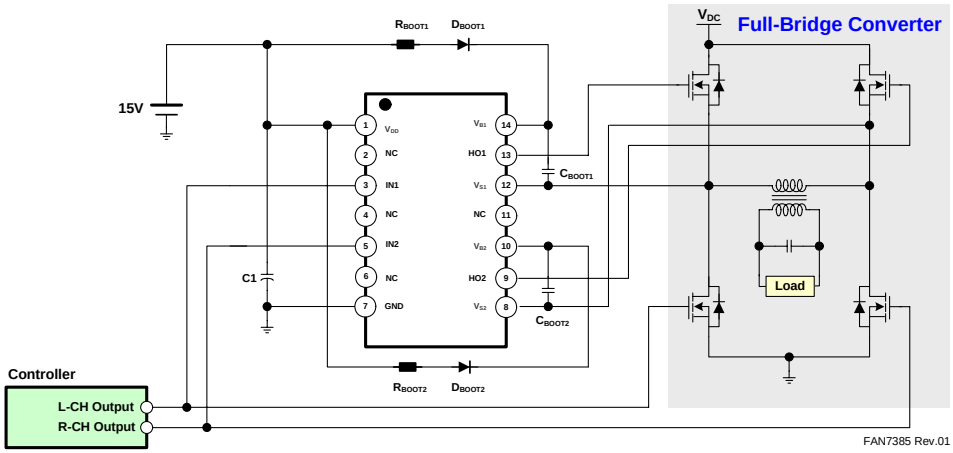


Figure 2. Full-Bridge Power Supply Application

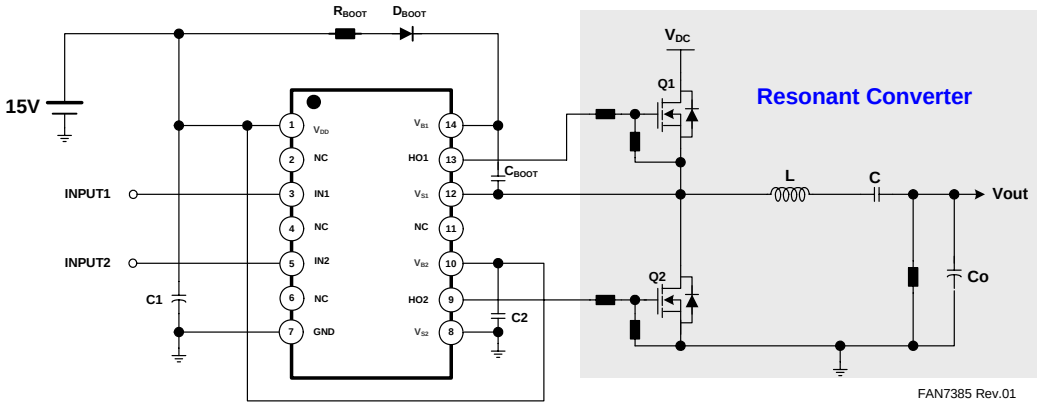


Figure 3. Half-Bridge LCC Resonant Converter Application

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Internal Block Diagram

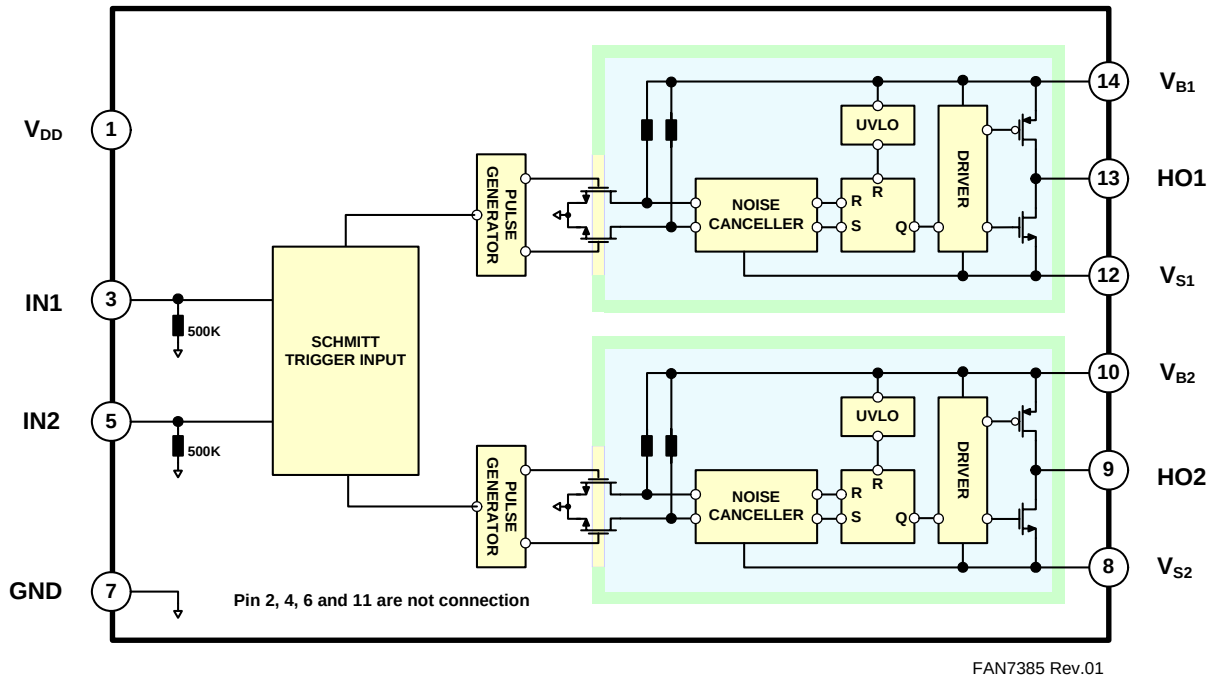


Figure 4. Functional Block Diagram

Pin Configuration

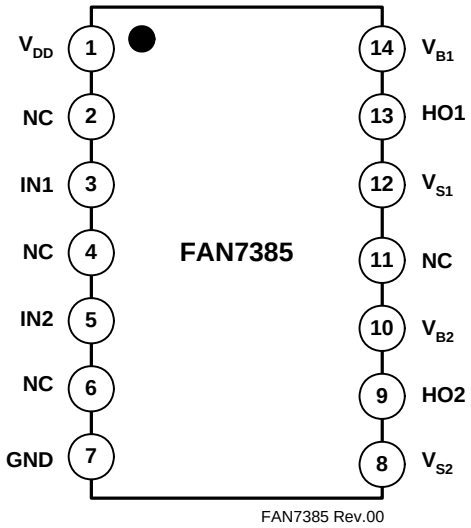


Figure 5. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	V_{DD}	Power supply
2	NC	Not connection
3	IN1	Channel 1 control input
4	NC	Not connection
5	IN2	Channel 2 control input
6	NC	Not connection
7	GND	Ground
8	V_{S2}	Channel 2 floating supply return
9	HO2	Channel 2 output
10	V_{B2}	Channel 2 floating supply
11	NC	Not connection
12	V_{S1}	Channel 1 floating supply return
13	HO1	Channel 1 output
14	V_{B1}	Channel 1 floating supply

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A=25°C, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
V_S	High-side offset voltage V_{S1}, V_{S2}	V_B-25	V_B+0.3	V
V_B	High-side floating supply voltage V_{B1}, V_{B2}	-0.3	625	V
V_{HO}	High-side floating output voltage H_{O1}, H_{O2}	V_S-0.3	V_B+0.3	V
V_{DD}	Low-side and logic-fixed supply voltage	-0.3	25	V
V_{IN}	Logic input voltage (IN1, IN2)	-0.3	V_{DD}+0.3	V
GND	Logic ground	V_{DD}-25	V_{DD}+0.3	V
dV_S/dt	Allowable offset voltage slew rate		50	V/ns
P_D[(2)(3)(4)]	Power dissipation		1.0	W
θ_{JA}	Thermal resistance, junction-to-ambient		110	°C/W
T_J	Junction temperature		150	°C
T_S	Storage temperature		150	°C

Notes:

2. Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
3. Refer to the following standards:
   JESD51-2: Integral circuits thermal test method environmental conditions - natural convection
   JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
4. Do not exceed P_D under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Condition	Min.	Max.	Unit
V_B	High-side floating supply voltage		V_S+10	V_S+20	V
V_S	High-side floating supply offset voltage		6-V_{DD}	600	V
V_{DD}	Supply voltage		10	20	V
V_{HO}	High-side (HO1, HO2) output voltage		V_S	V_B	V
V_{IN}	Logic input voltage (IN1, IN2)		GND	V_{DD}	V
T_A	Ambient temperature		-40	125	°C

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Electrical Characteristics

V_{BIAS} (V_{DD}, V_{BS1}, V_{BS2}) = 15.0V, T_A = 25°C, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND. The V_O and I_O parameters are referenced to V_{S1} and V_{S2} and are applicable to the respective outputs HO1 and HO2.

Symbol	Characteristics	Condition	Min.	Typ.	Max.	Unit
SUPPLY CURRENT SECTION						
I_{QDD}	Quiescent V_{DD} supply current	V_{IN1}=V_{IN2}=0V or 5V		28	50	µA
I_{PDD}	Operating V_{DD} supply current	f_{IN1}=f_{IN2}=10kHz, rms value		35	70	µA
BOOTSTRAPPED POWER SUPPLY SECTION						
V_{BSUV+}	V_{BS1} and V_{BS2} supply under-voltage positive going threshold	V_{BS1}=V_{BS2}=Sweep	8.2	9.1	10.2	V
V_{BSUV-}	V_{BS1} and V_{BS2} supply under-voltage negative going threshold	V_{BS1}=V_{BS2}=Sweep	7.6	8.5	9.6	V
V_{BSHYS}	V_{BS1} and V_{BS2} supply under-voltage lockout hysteresis	V_{BS1}=V_{BS2}=Sweep		0.6		V
I_{LK}	Offset supply leakage current	V_B=V_S=600V			10	µA
$I_{QBS1,2}$	Quiescent V_{BS1} and V_{BS2} supply current	V_{IN1}=0V or 5V		50	85	µA
$I_{PBS1,2}$	Operating V_{BS1} and V_{BS2} supply current	f_{IN1}=10kHz, rms value		220	300	µA
GATE DRIVER OUTPUT SECTION						
V_{OH}	High-level output voltage, V_{BIAS}-V_O	I_O=0mA (No Load)			30	mV
V_{OL}	Low-level output voltage, V_O	I_O=0mA (No Load)			30	mV
I_{O+}	Output HIGH short-circuit pulse current	V_O=0V, V_{IN}=5V with PW<10µs	250	350		mA
I_{O-}	Output LOW short-circuit pulsed current	V_O=15V, V_{IN}=0V with PW<10µs	500	650		mA
V_S	Allowable negative V_S pin voltage for IN signal propagation to H_O			-9.8	-7.0	V
LOGIC INPUT SECTION (IN1 AND IN2)						
V_{IH}	Logic "1" input voltage		2.5			V
V_{IL}	Logic "0" input voltage				1.3	V
I_{IN+}	Logic "1" input bias current	V_{IN}=5V		10	20	µA
I_{IN-}	Logic "0" input bias current	V_{IN}=0V			2.0	µA
R_{IN}	Input pull-down resistance		400	500	600	KΩ

Dynamic Electrical Characteristics

T_A=25°C, V_{BIAS} (V_{DD}, V_{BS1}, V_{BS2}) = 15.0V, V_{S1} = V_{S2} = GND, C_{Load} = 1000pF unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	V_S=0V		110	180	ns
t_{off}	Turn-off propagation delay	V_S=0V or 600V[5]		110	180	ns
t_r	Turn-on rise time			50	90	ns
t_f	Turn-off fall time			30	70	ns
MT	Delay matching, Channel 1 & 2 turn-on/off			0		ns

Notes:

5. This parameter guaranteed by design.

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Typical Characteristics

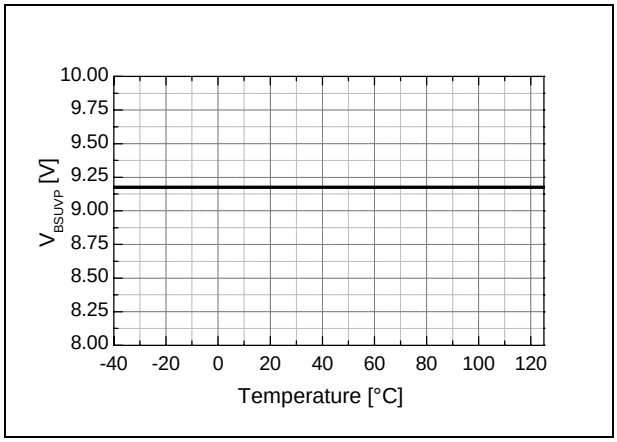


Figure 6. V_{BS} UVLO (+) vs. Temperature

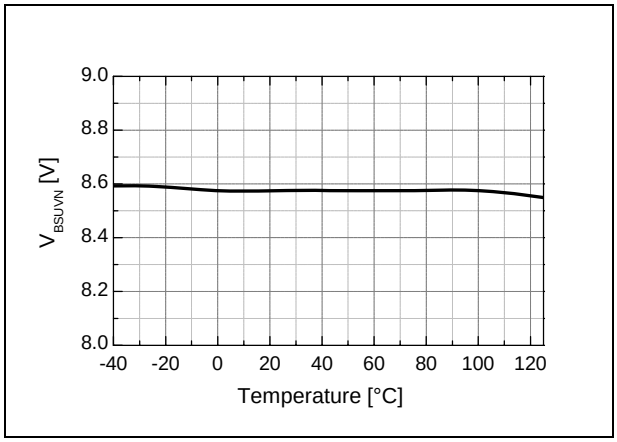


Figure 7. V_{BS} UVLO (-) vs. Temperature

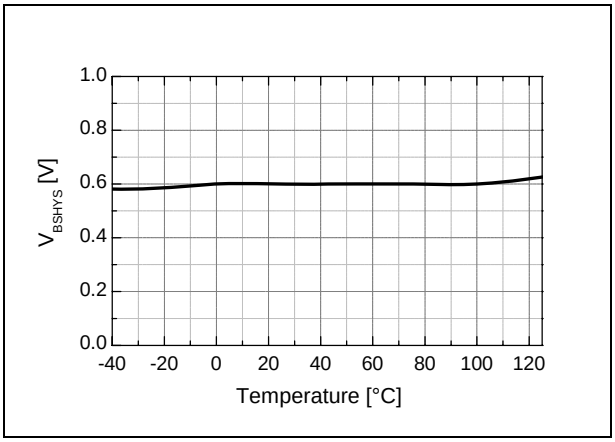


Figure 8. V_{BS} UVLO Hysteresis vs. Temperature

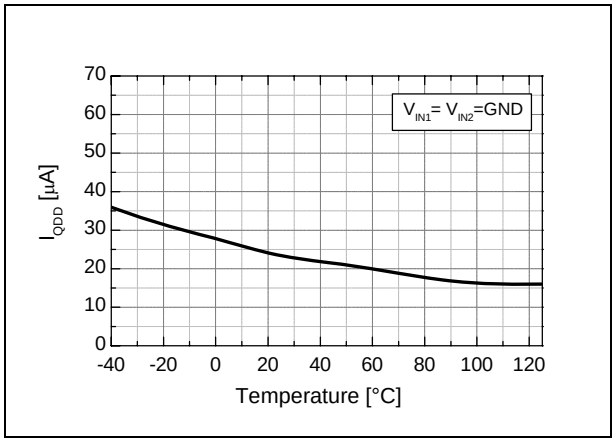


Figure 9. V_{DD} Quiescent Current vs. Temperature

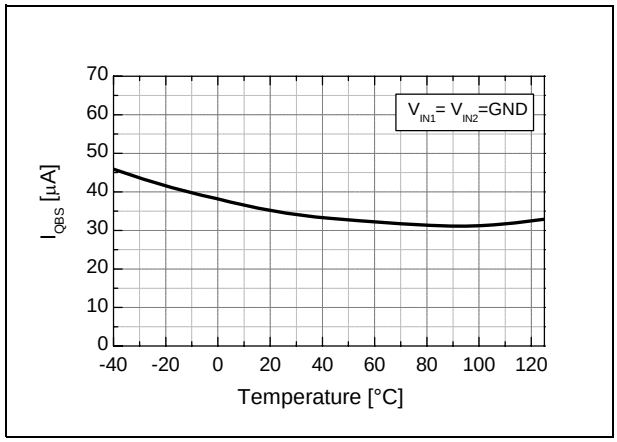


Figure 10. V_{BS} Quiescent Current vs. Temperature

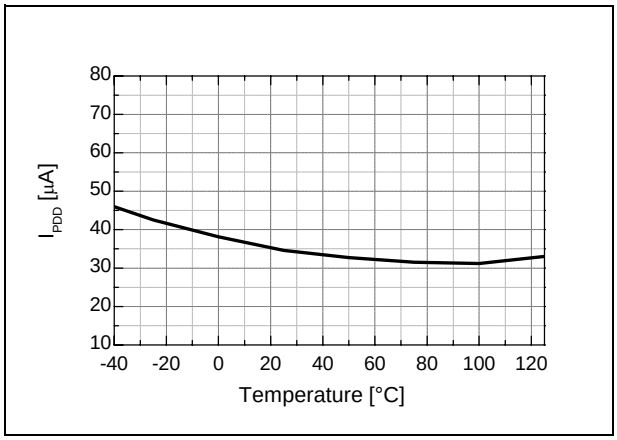


Figure 11. V_{DD} Operating Current vs. Temperature

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Typical Characteristics (Continued)

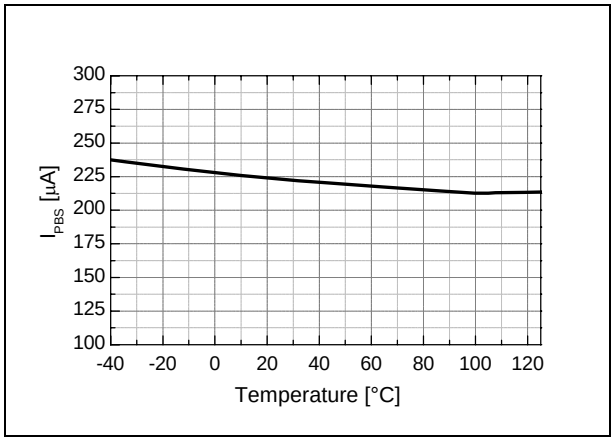


Figure 12. V_{BS} Operating Current vs. Temperature

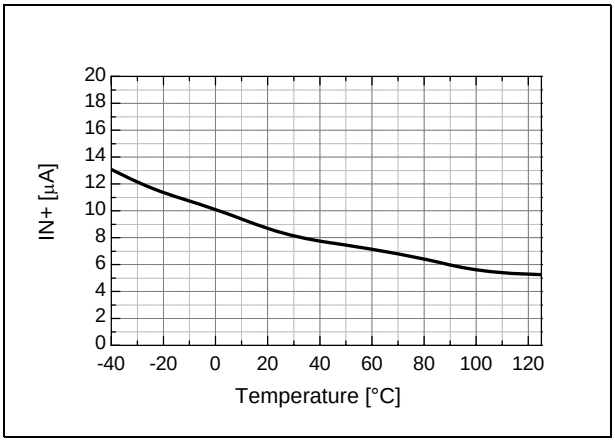


Figure 13. Logic High Input Current vs. Temperature

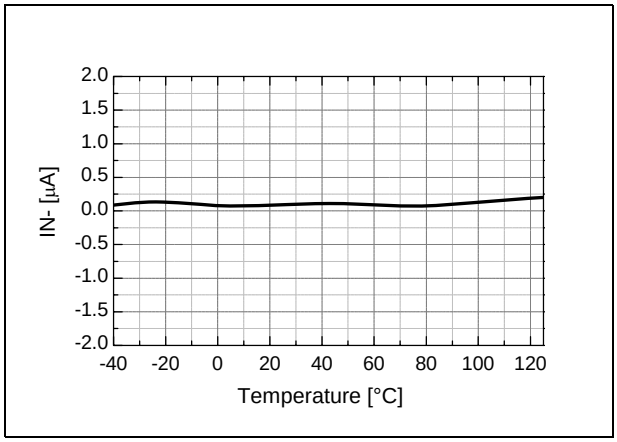


Figure 14. Logic Low Input Current vs. Temperature

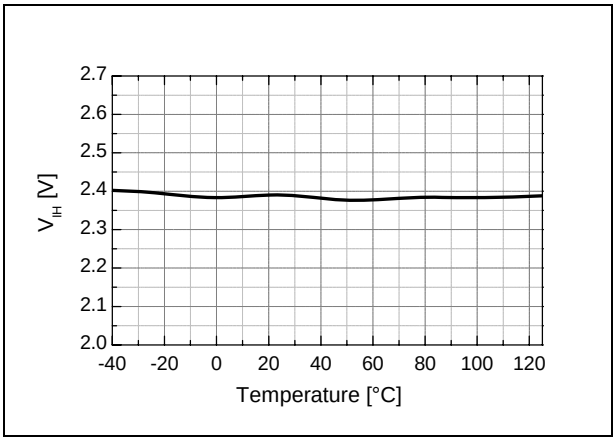


Figure 15. Logic Input High Voltage vs. Temperature

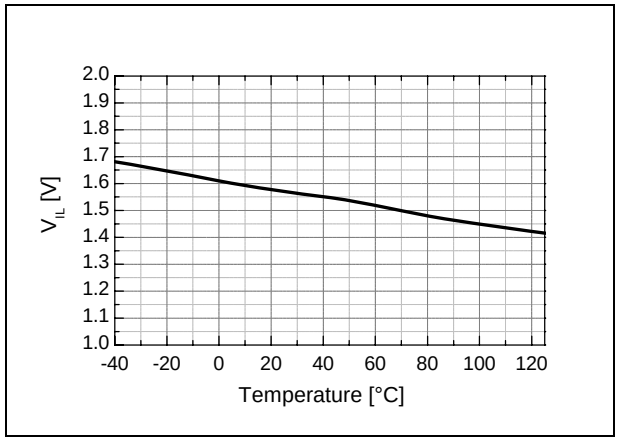


Figure 16. Logic Input Low Voltage vs. Temperature

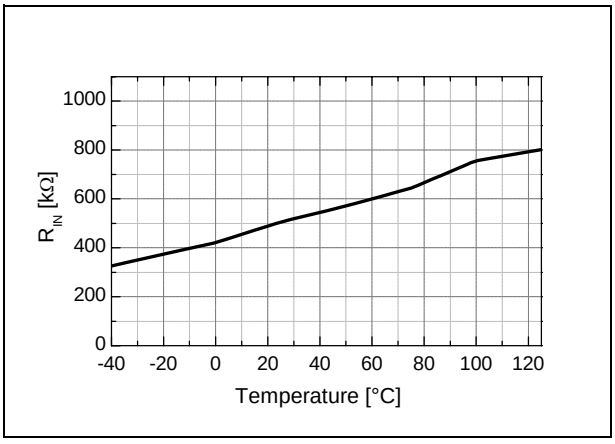


Figure 17. Logic Input Resistance vs. Temperature

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Typical Characteristics (Continued)

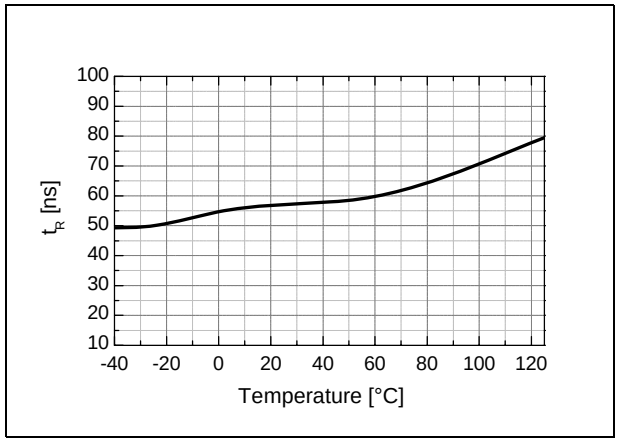


Figure 18. Rising Time vs. Temperature

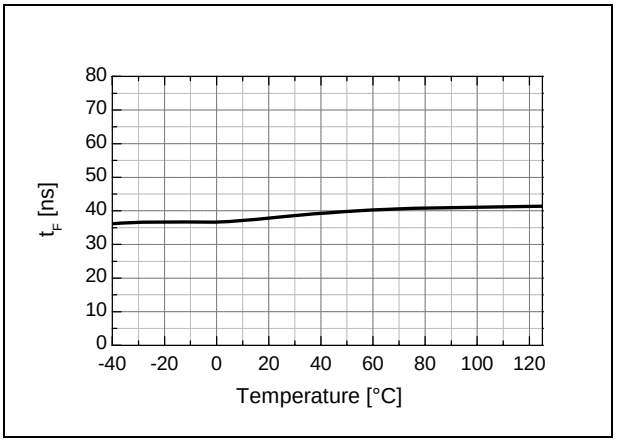


Figure 19. Falling Time vs. Temperature

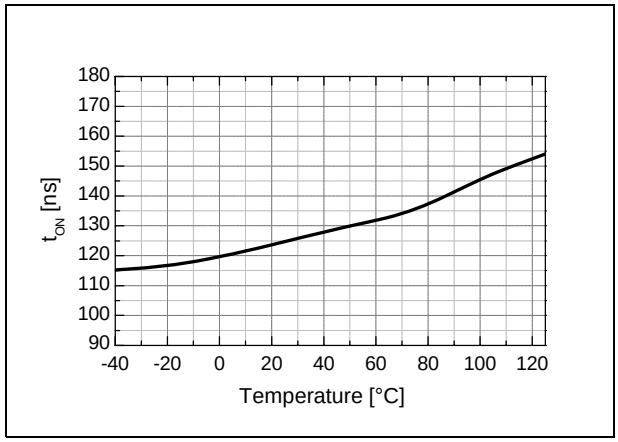


Figure 20. Turn-On Delay Time vs. Temperature

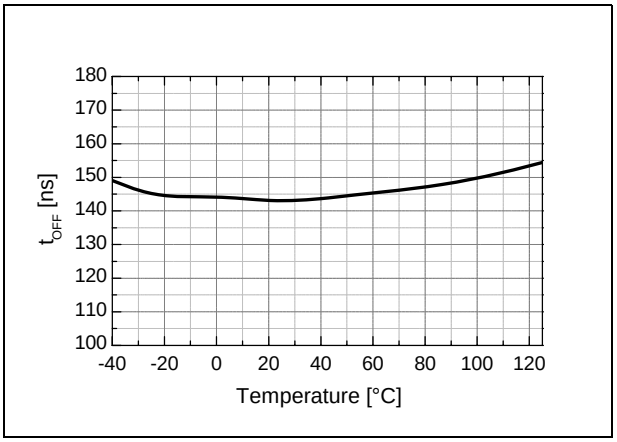


Figure 21. Turn-Off Delay Time vs. Temperature

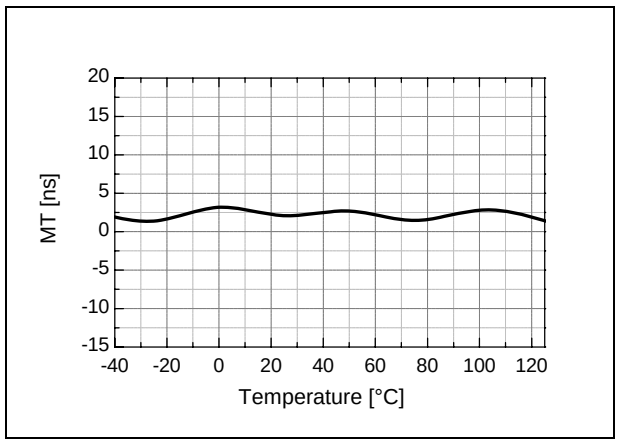


Figure 22. Delay Matching Time vs. Temperature

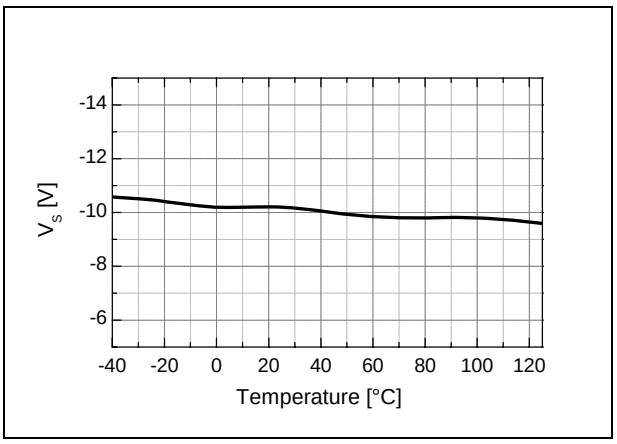


Figure 23. Allowable Negative V_S Voltage for Signal Propagation to High Side vs. Temperature

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Typical Characteristics (Continued)

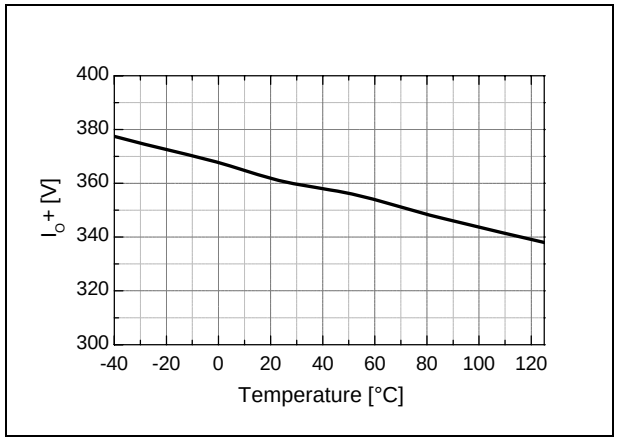


Figure 24. Output High Short-Circuit Pulse Current vs. Temperature

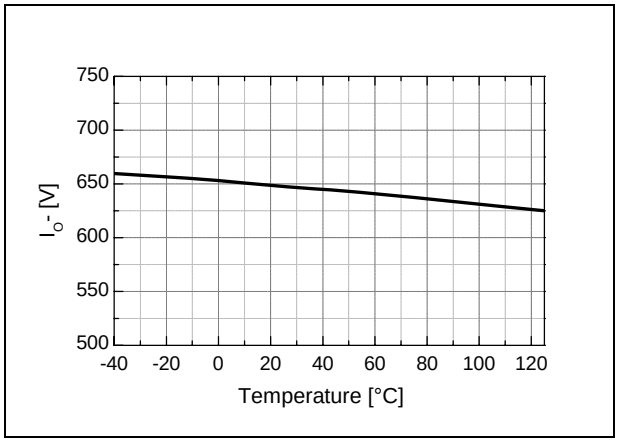


Figure 25. Output Low Short-Circuit Pulse Current vs. Temperature

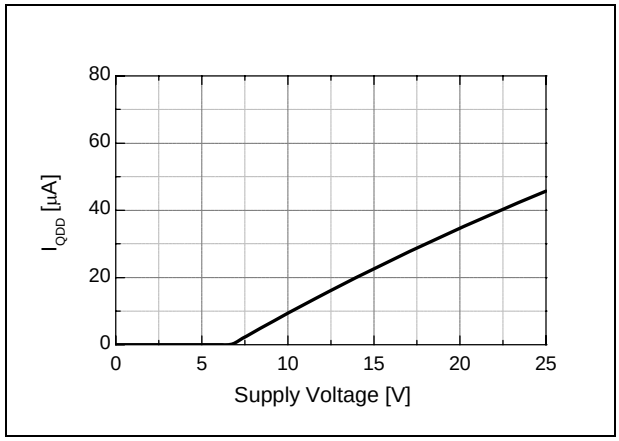


Figure 26. V_{DD} Quiescent Current vs. Supply Voltage

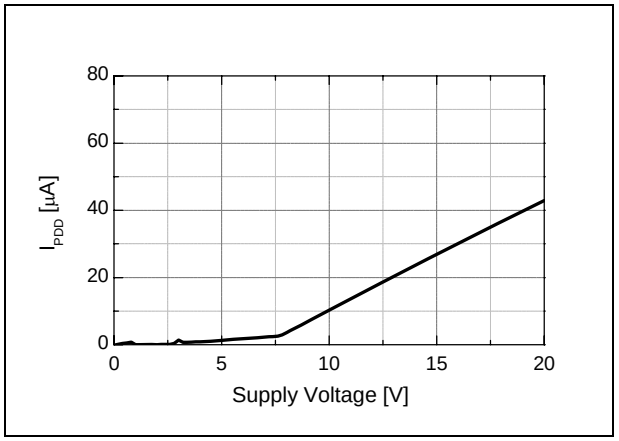


Figure 27. V_{DD} Operating Current vs. Supply Voltage

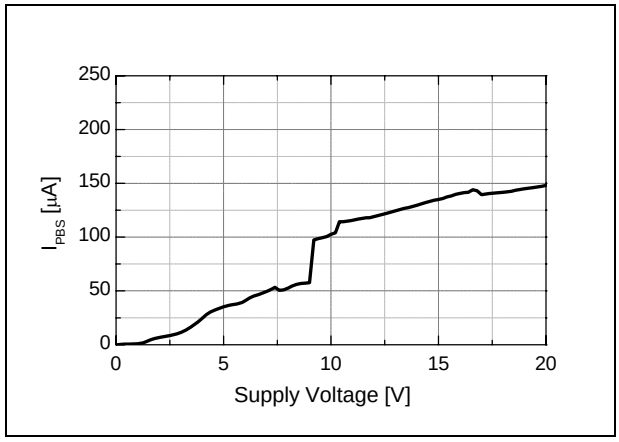


Figure 28. V_{BS} Operating Current vs. Supply Voltage

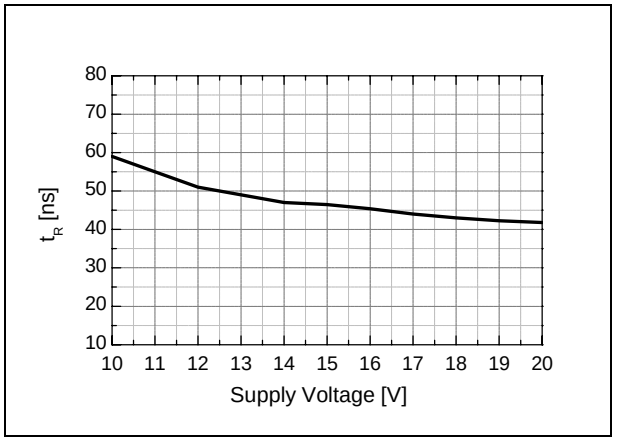


Figure 29. Rising Time vs. Supply Voltage

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Typical Characteristics (Continued)

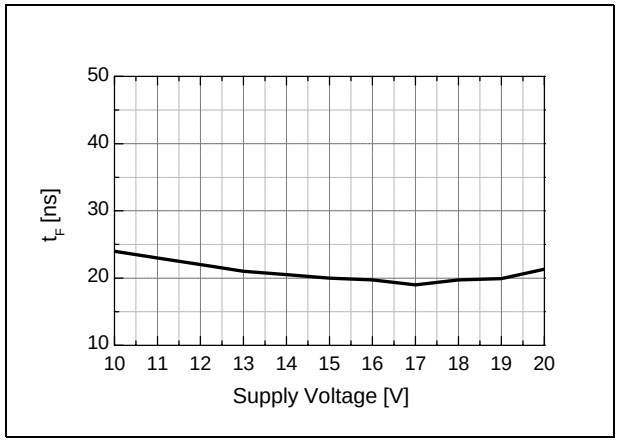


Figure 30. Falling Time vs. Supply Voltage

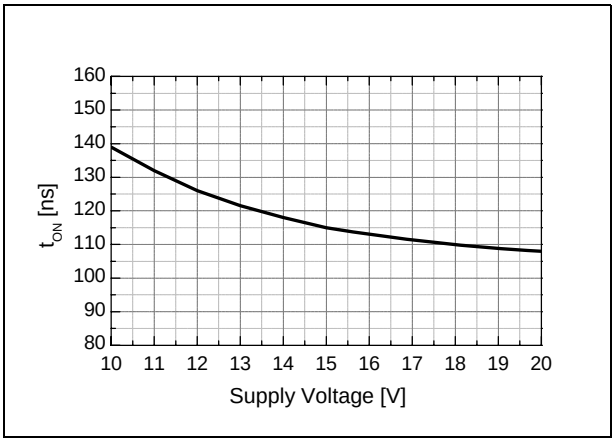


Figure 31. Turn-On Delay Time vs. Supply Voltage

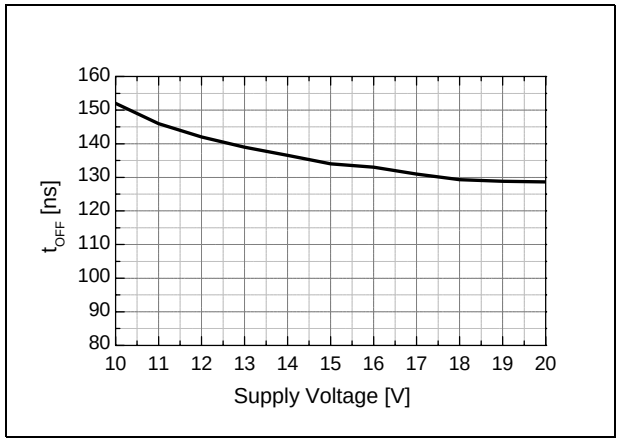


Figure 32. Turn-Off Delay Time vs. Supply Voltage

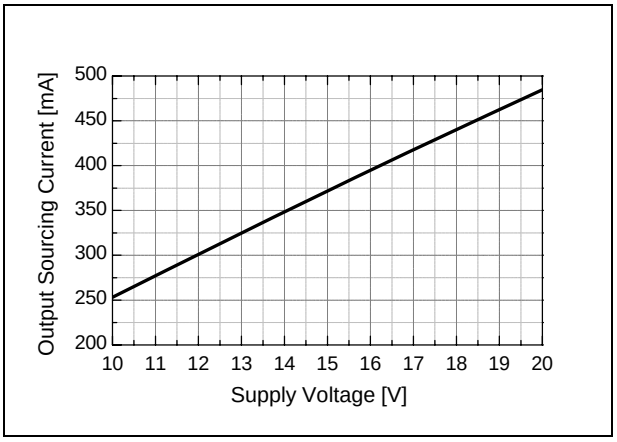


Figure 33. Output Source Current vs. Supply Voltage

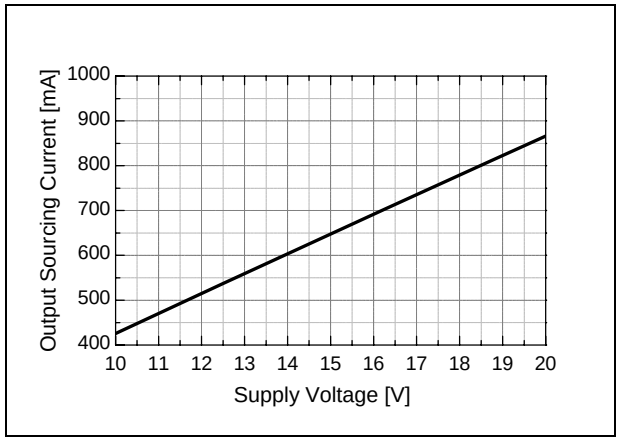


Figure 34. Output Sink Current vs. Supply Voltage

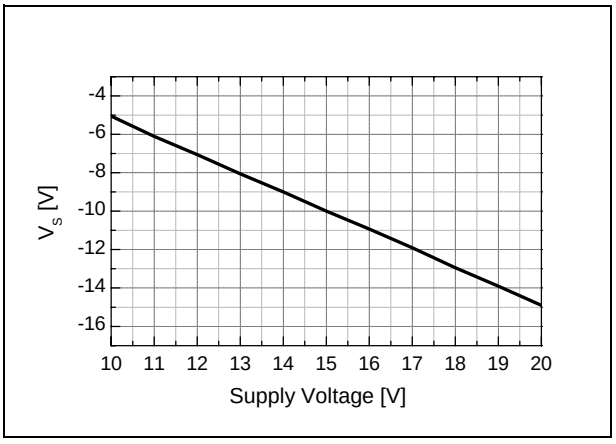


Figure 35. Allowable Negative V_S Voltage for Signal Propagation to High Side vs. Supply Voltage

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Switching Time Definitions

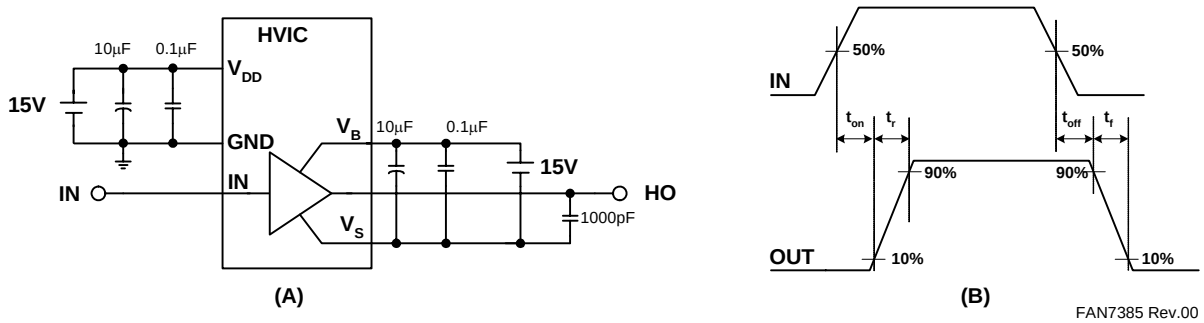


Figure 36. Switching Time Test Circuit

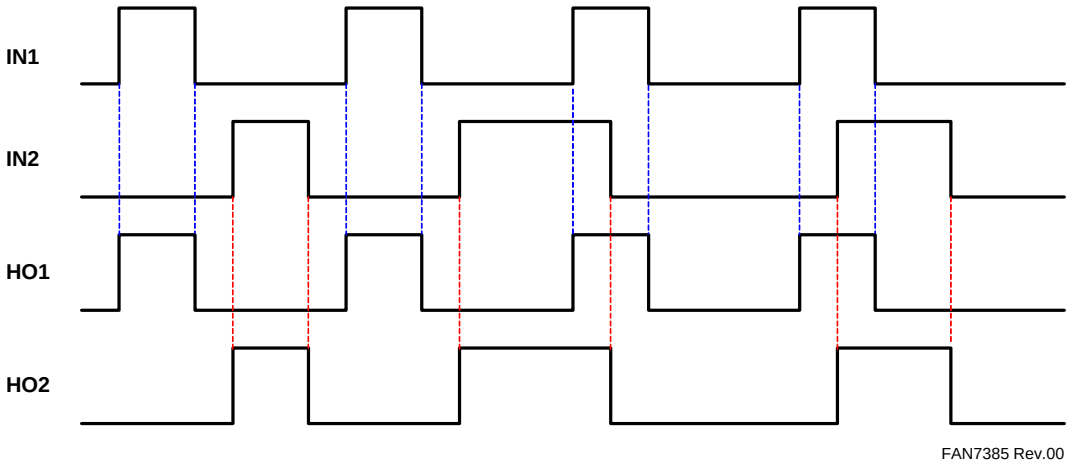


Figure 37. Input / Output Waveforms

Typical Application Information

1. Under-Voltage Lockout (UVLO)

The FAN7385 has an under-voltage lockout (UVLO) protection circuit to prevent malfunction when V_{BS1} and V_{BS2} are lower than the specified threshold voltage. The UVLO circuit monitors the bootstrap capacitor voltages ($V_{BS1,}$ V_{BS2}) independently.

2. Layout Consideration

For optimum performance, considerations must be given during printed circuit board (PCB) layout.

2.1 Supply Capacitors

If the output stages are able to quickly turn on a switching device with a high current value, the supply capacitors must be placed as close as possible to the device pins (V_{DD} and GND for the ground-tied supply, V_B and V_S for the floating supply) to minimize parasitic inductance and resistance.

2.2 Gate Drive Loop

Current loops behave like antennae, able to receive and transmit noise. To reduce the noise coupling/emission and improve the power switch turn-on and off performances, gate drive loops must be reduced as much as possible.

2.3 Ground Plane

To minimize noise coupling, avoid placing the ground plane under or near the high-voltage floating side.

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Package Dimensions

14-SOP

Dimensions are in millimeters unless otherwise noted.

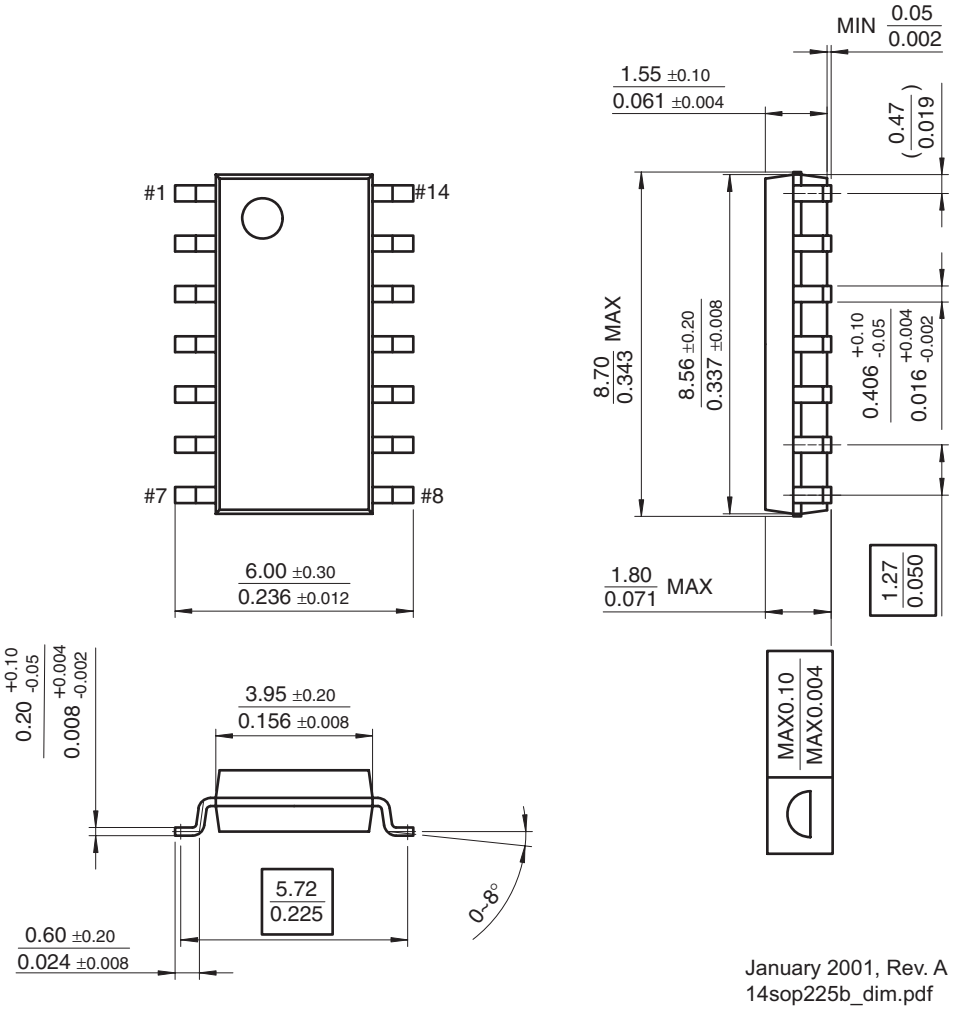


Figure 38. 14-Lead Small Outline Package (SOP)

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